

An aerial photograph of the Fermilab facility, showing a large circular accelerator ring, various buildings, and surrounding green fields. The title text is overlaid on a white box in the top left corner.

# A Low-Power Wave Union TDC Implemented in FPGA

Wu, Jinyuan

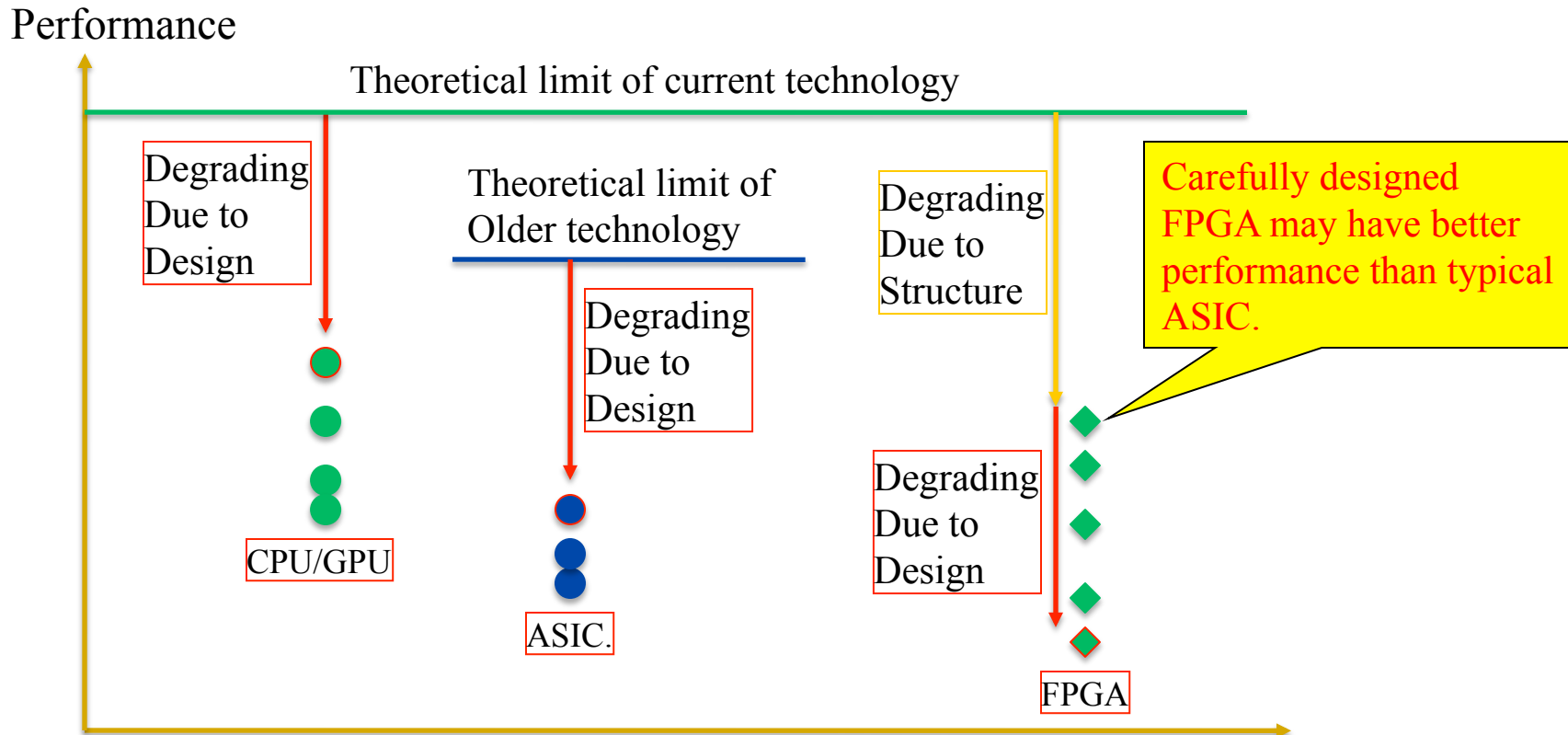
Fermilab

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Illinois Mathematics and Science Academy

Sept. 2011

# Performance Degrading in CPU/GPU, ASIC & FPGA



- Imperfect designs degrade performance of ICs, including CPU/GPU considerably.
- ASIC devices are built using older technology and suffering similar design degrading.
- FPGA internal structure causes extra performance degrading in addition to design degrading.
- Design modification in FPGA is easier so that design degrading can be minimized.

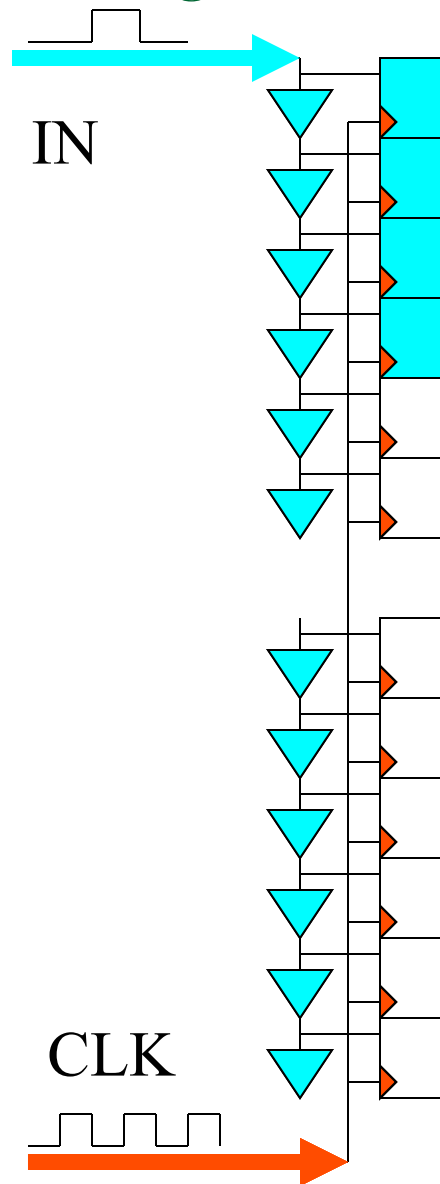
## Introduction

- A 32-channel Wave Union TDC firmware has been implemented in an Altera Cyclone III FPGA device (EP3C25F324C6N, \$73.90) and has been tested on a Cyclone III evaluation card.
- Low-power design practice has been applied for applications in vacuum.
- Time measurement function is tested on 16 channels and typical  $\Delta t$  RMS resolution between two channels is 25-30 ps.
- Power consumption is measured for 32 channels at  $\sim 27$  mW/channel.

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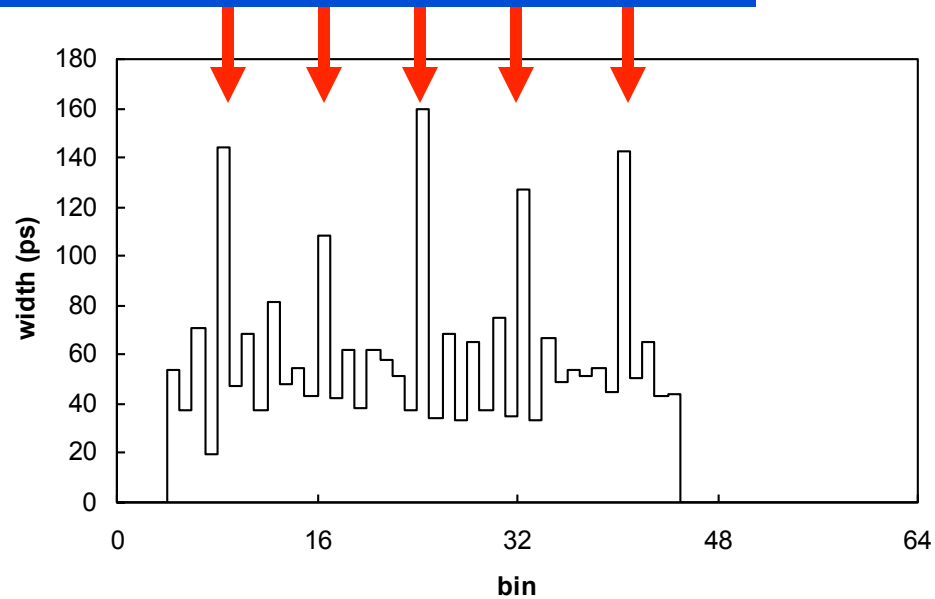
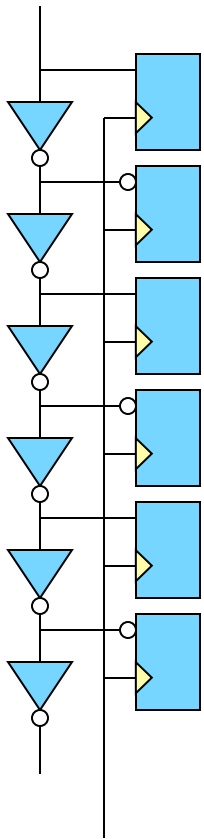
# The Wave Union TDC Implemented in FPGA

## TDC Using FPGA Logic Chain Delay

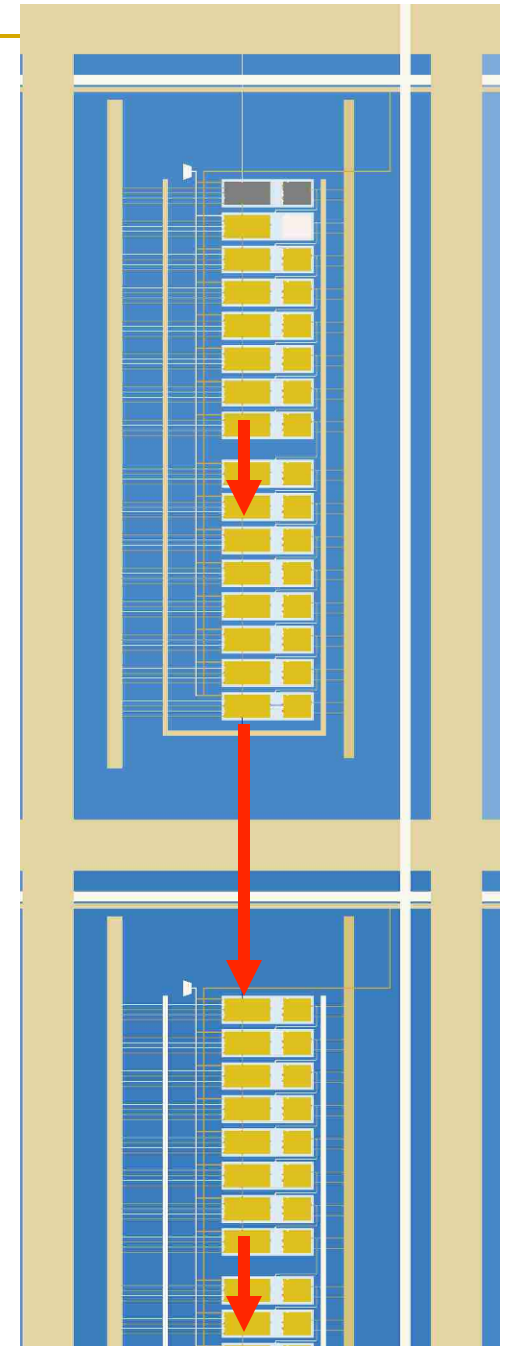


- This scheme uses current FPGA technology ☺
- Low cost chip family can be used. (e.g. EP2C8T144C6 \$31.68) ☺
- Fine TDC precision can be implemented in slow devices (e.g., 20 ps in a 400 MHz chip). ☺

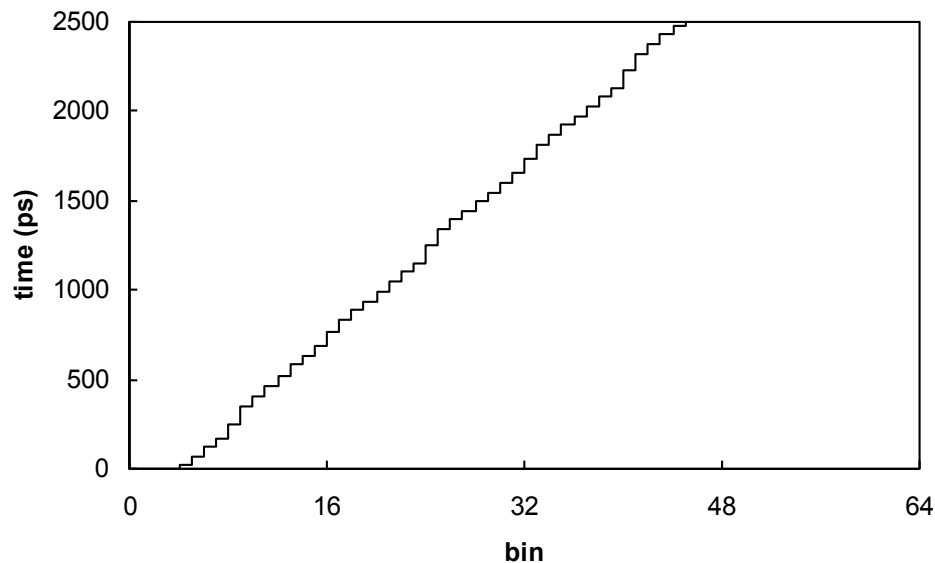
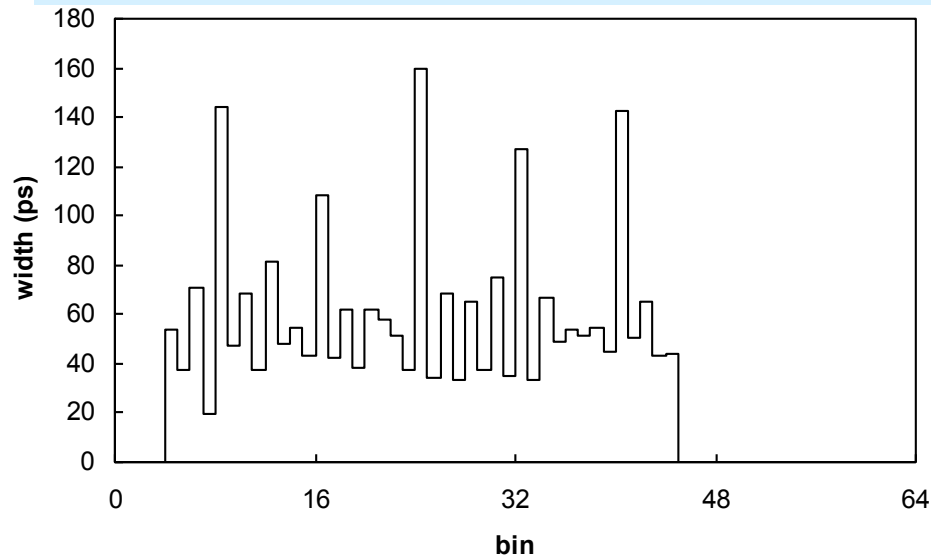
# Two Major Issues In a Free Operating FPGA



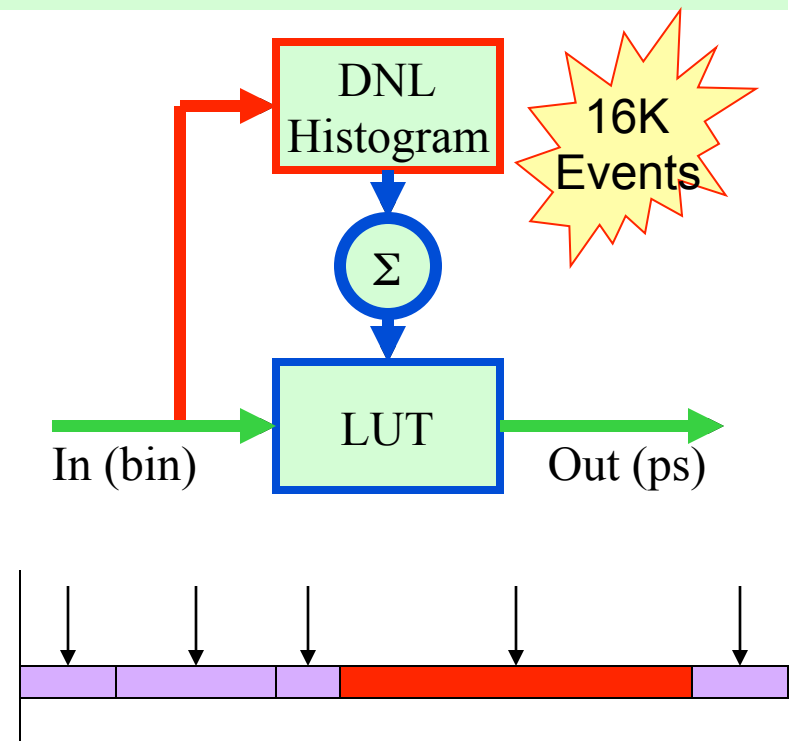
1. Widths of bins are different and varies with supply voltage and temperature.
2. Some bins are ultra-wide due to LAB boundary crossing



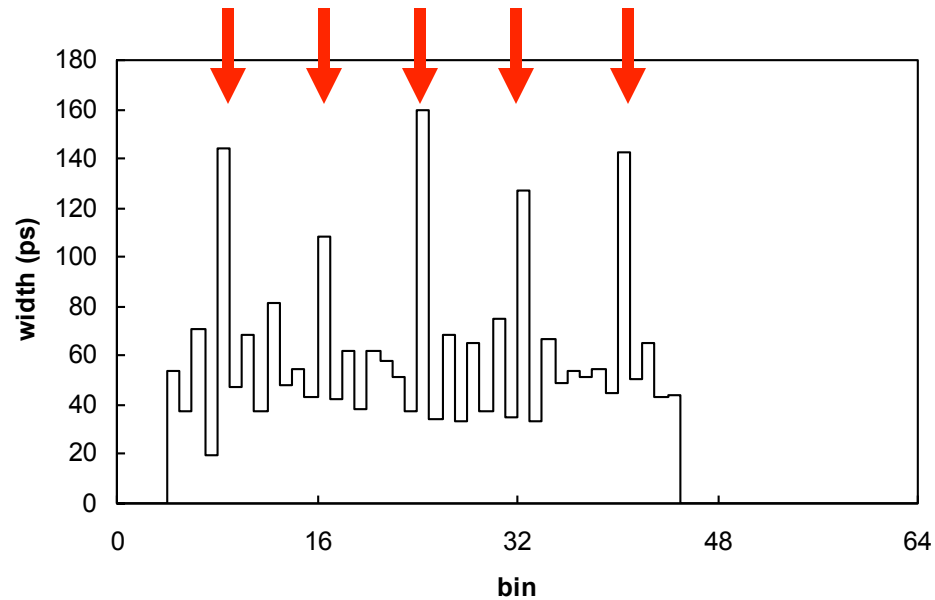
# Auto Calibration Using Histogram Method



- It provides a bin-by-bin calibration at certain temperature.
- It is a turn-key solution (bin in, ps out)
- It is semi-continuous (auto update LUT every 16K events)

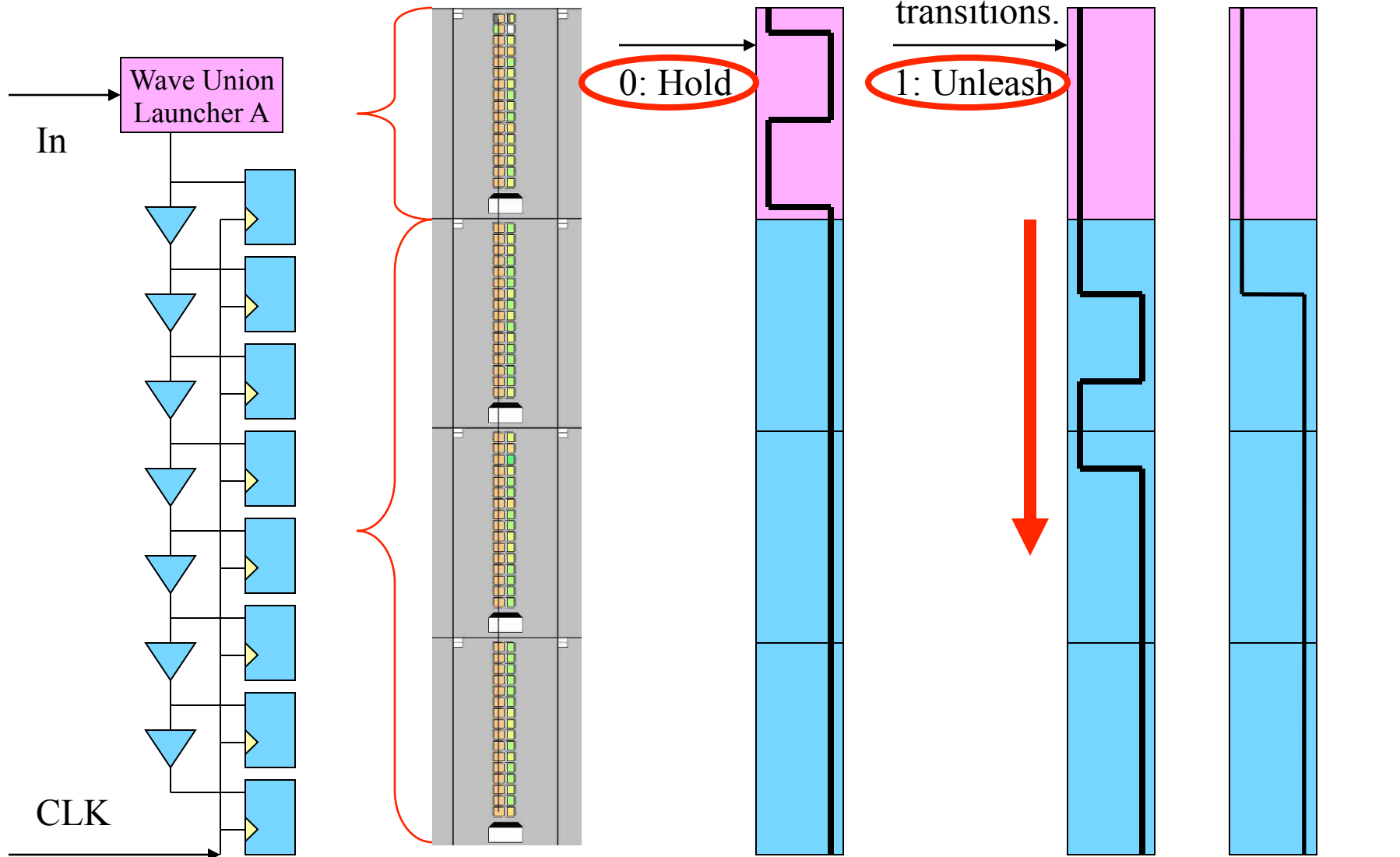


# Good, However

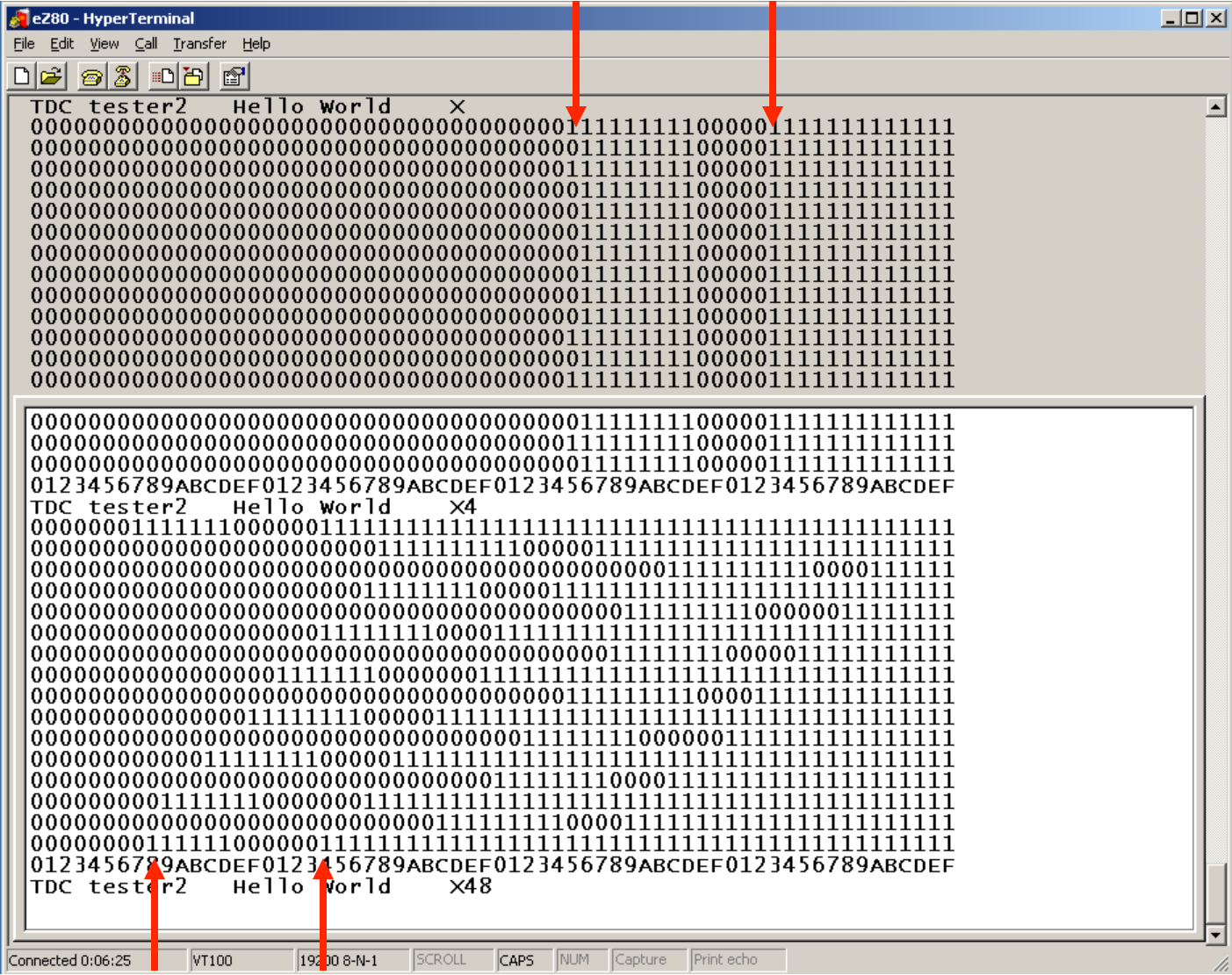


- Auto calibration solved some problems 😊
- However, it won't eliminate the ultra-wide bins 😞

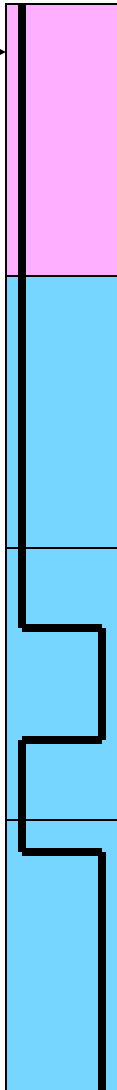
# Wave Union Launcher A



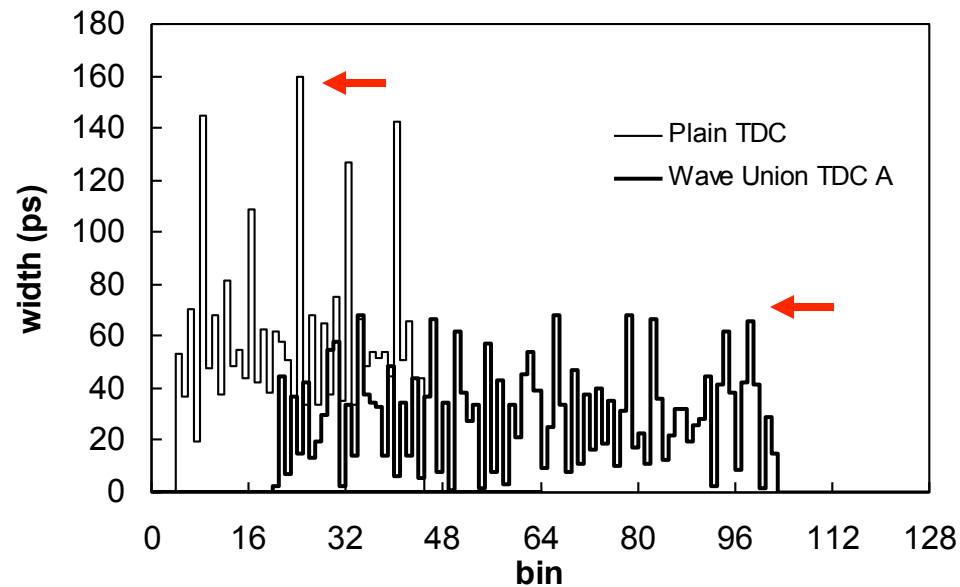
## Wave Union Launcher A: 2 *Measurements/hit*



# 1: Unleash



# Sub-dividing Ultra-wide Bins



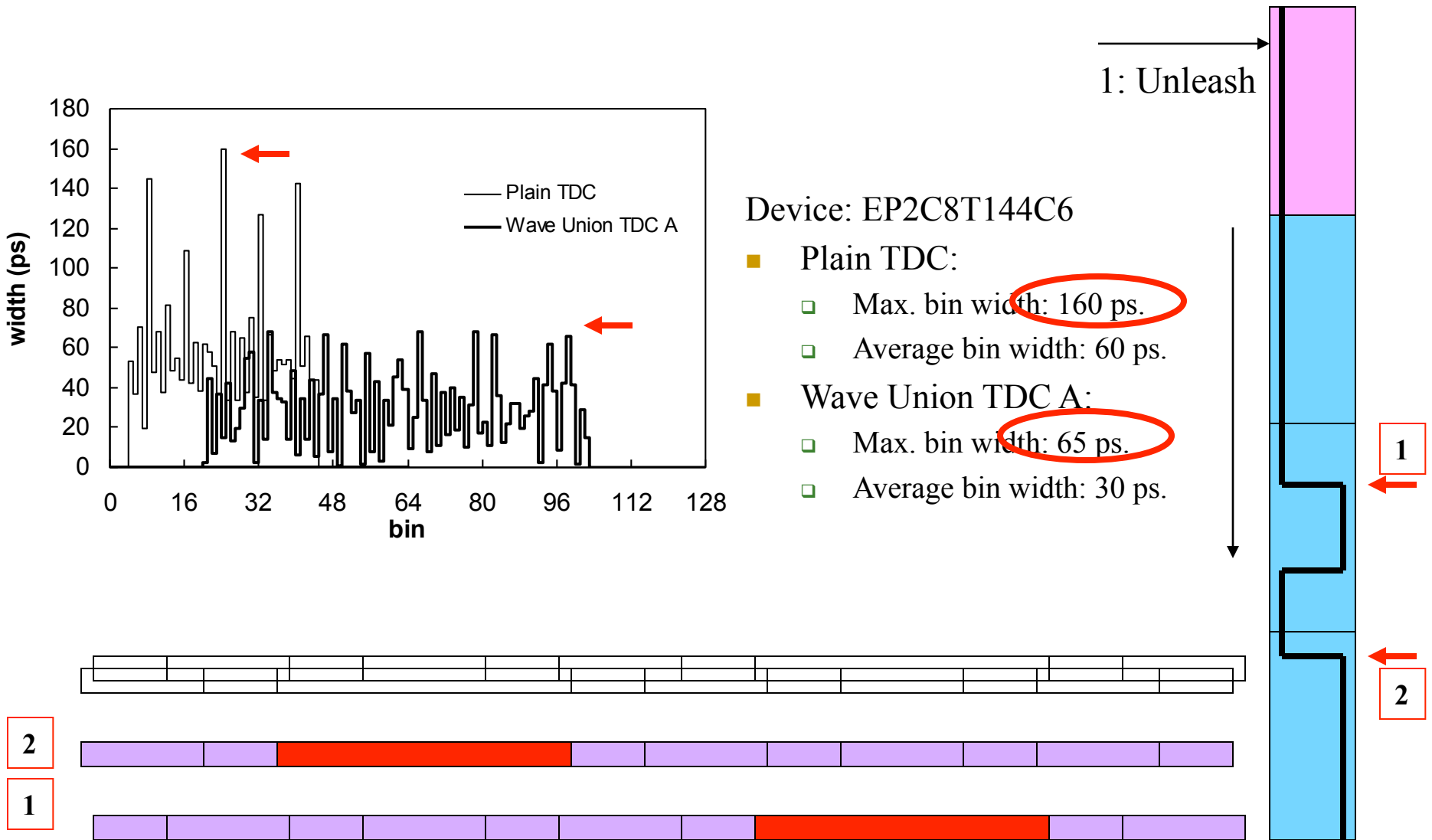
Device: EP2C8T144C6

## Plain TDC:

- Max. bin width: 160 ps.
- Average bin width: 60 ps.

## Wave Union TDC A:

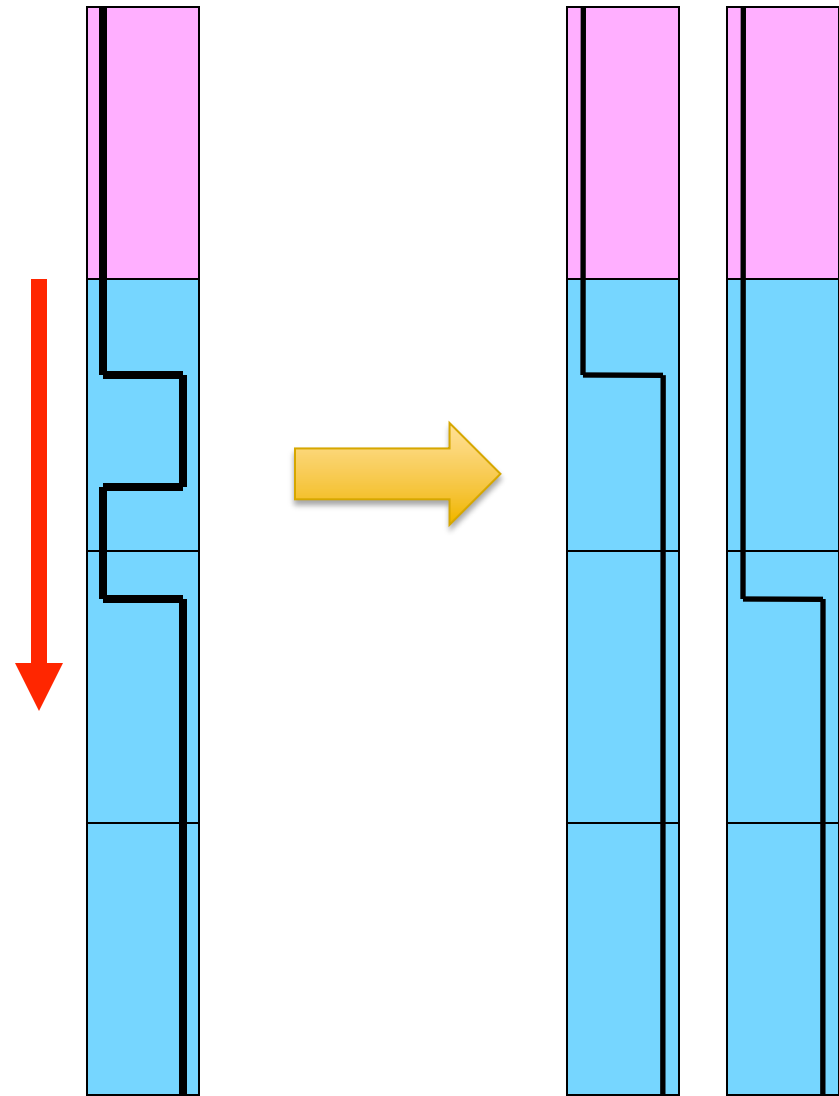
- Max. bin width: 65 ps.
- Average bin width: 30 ps.



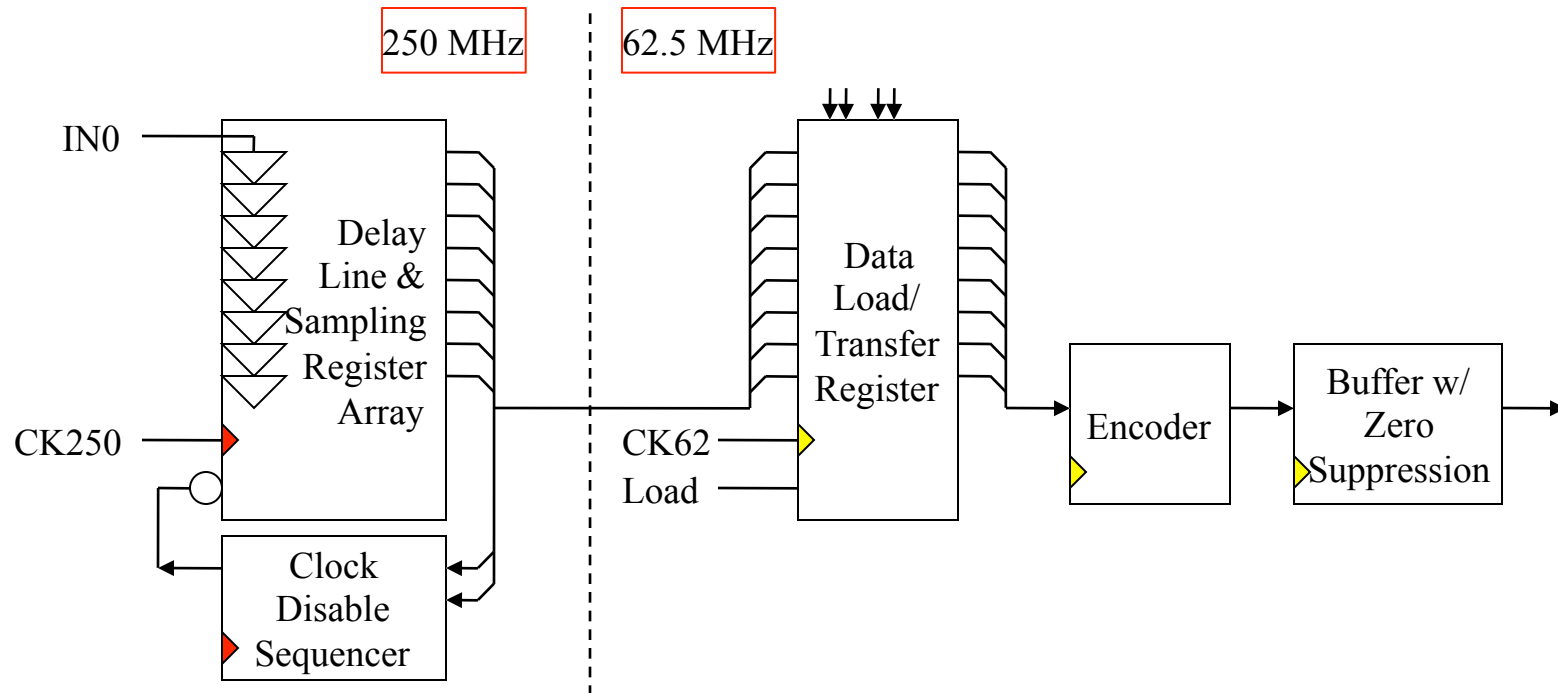
# Low-power Design Practices

# Low-Power Design Practice: Wave Union

- Intrinsically the Wave Union TDC is a low-power scheme.
- Multiple measurements are made with one set of delay line, register encoder etc. yielding finer resolution that otherwise needs several regular TDC blocks to achieve.

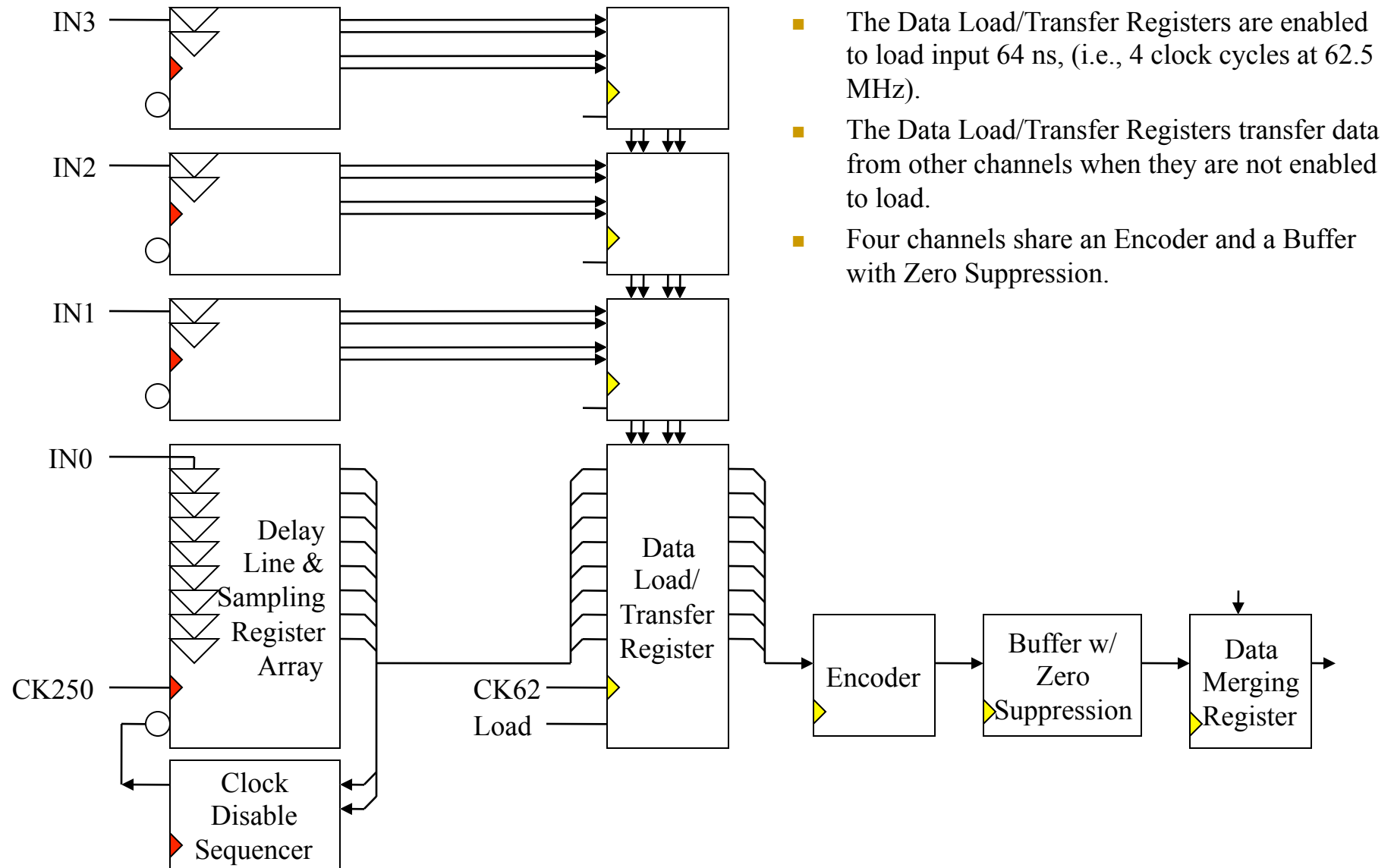


# Low-Power Design Practice: Clock Speed

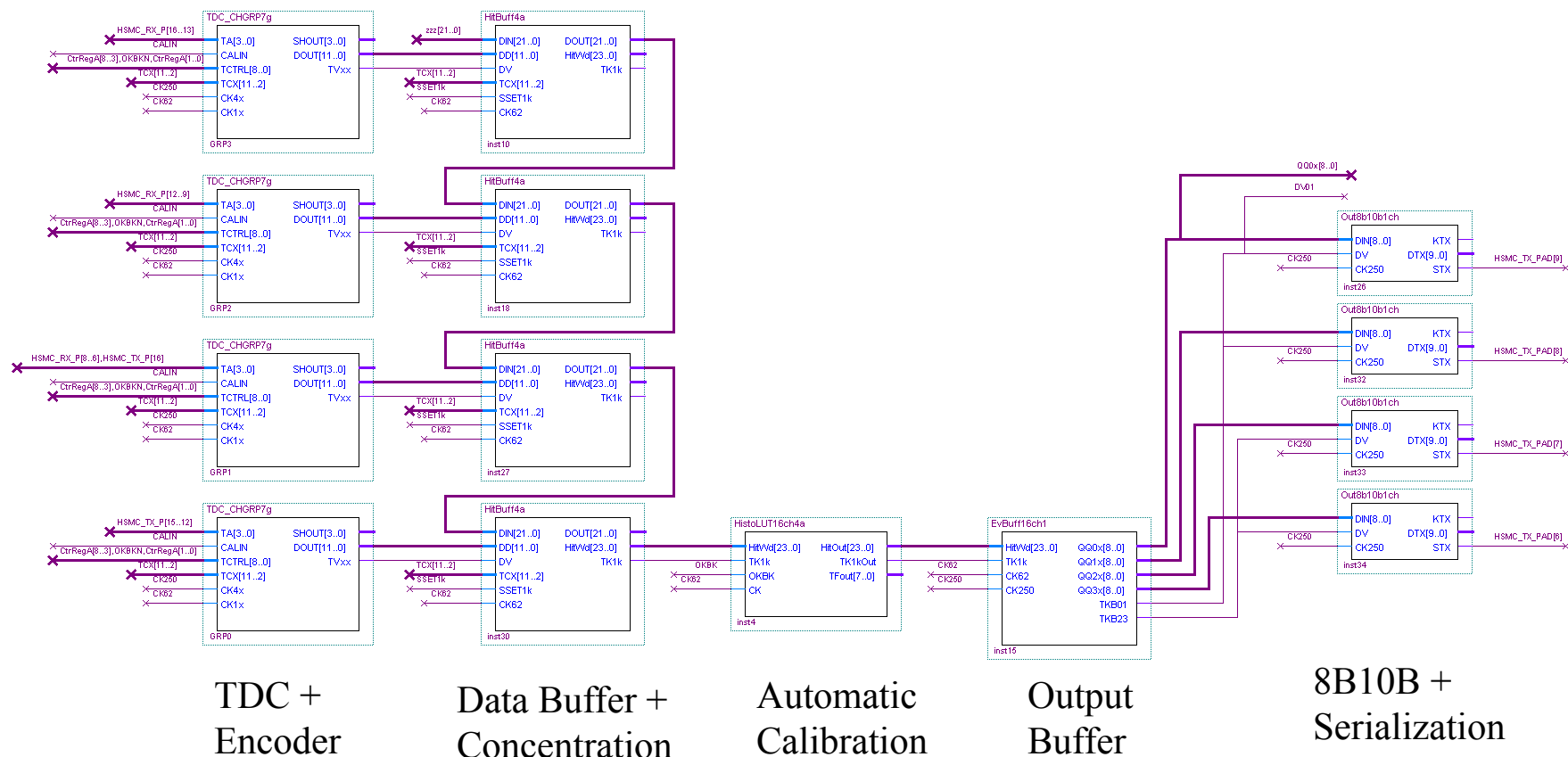


- The Sampling Register Arrays are clocked at 250 MHz.
- All other stages are clocked at 62.5 MHz.
- When a valid hit is sampled, the Sampling Register Array is disabled so that the registered pattern is stable for 64 ns.
- The Data Load/Transfer Registers are enabled to load input 64 ns, so that a valid hit is guaranteed to be load once and only once.

# Low Power Design Practice: Resource Sharing



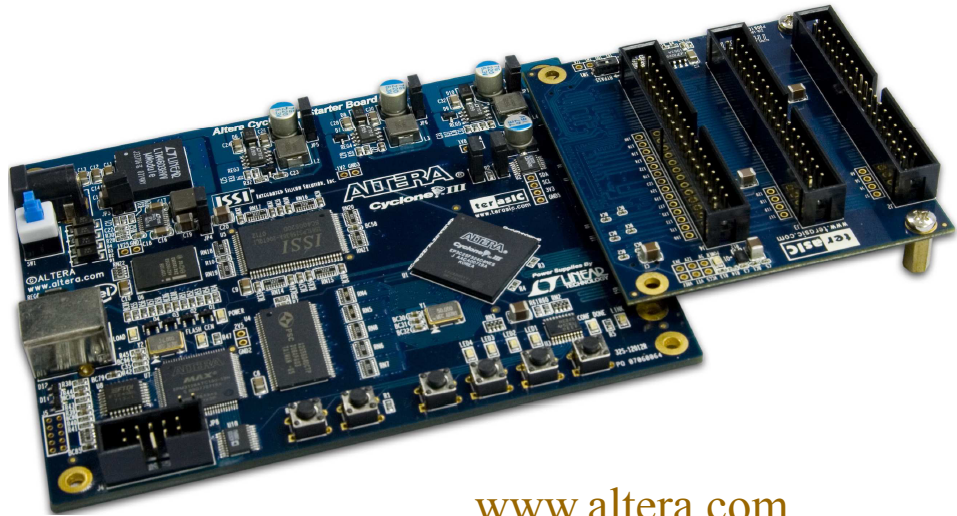
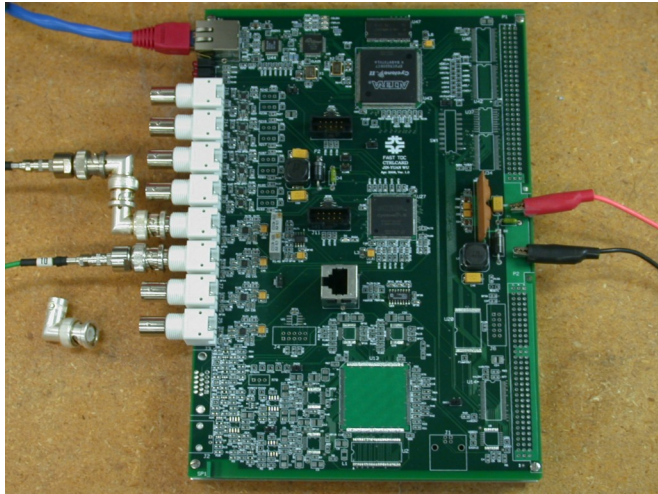
# Block Diagram of 16 Channels



- The hit time for each of the 16 channel inputs is digitized and encoded.
- Data from 4 channels are buffered and data from 4 groups of 4 channels are merged together.
- Raw hit times are converted to fine time through automatic calibration block.
- Data from all 16 channels are buffered and sent out via 4 pairs of LVDS ports @250 M bits/s.

# Test Results

# The Test Hardware



[www.altera.com](http://www.altera.com)

2008

Altera Cyclone II + VME (~\$1k)

FPGA: EP2C8T144C6 (\$28.80)

16 channel: 25 ps

2 channel: 10 ps

81 mW/channel

Ref: Search “Wave Union TDC”

2011

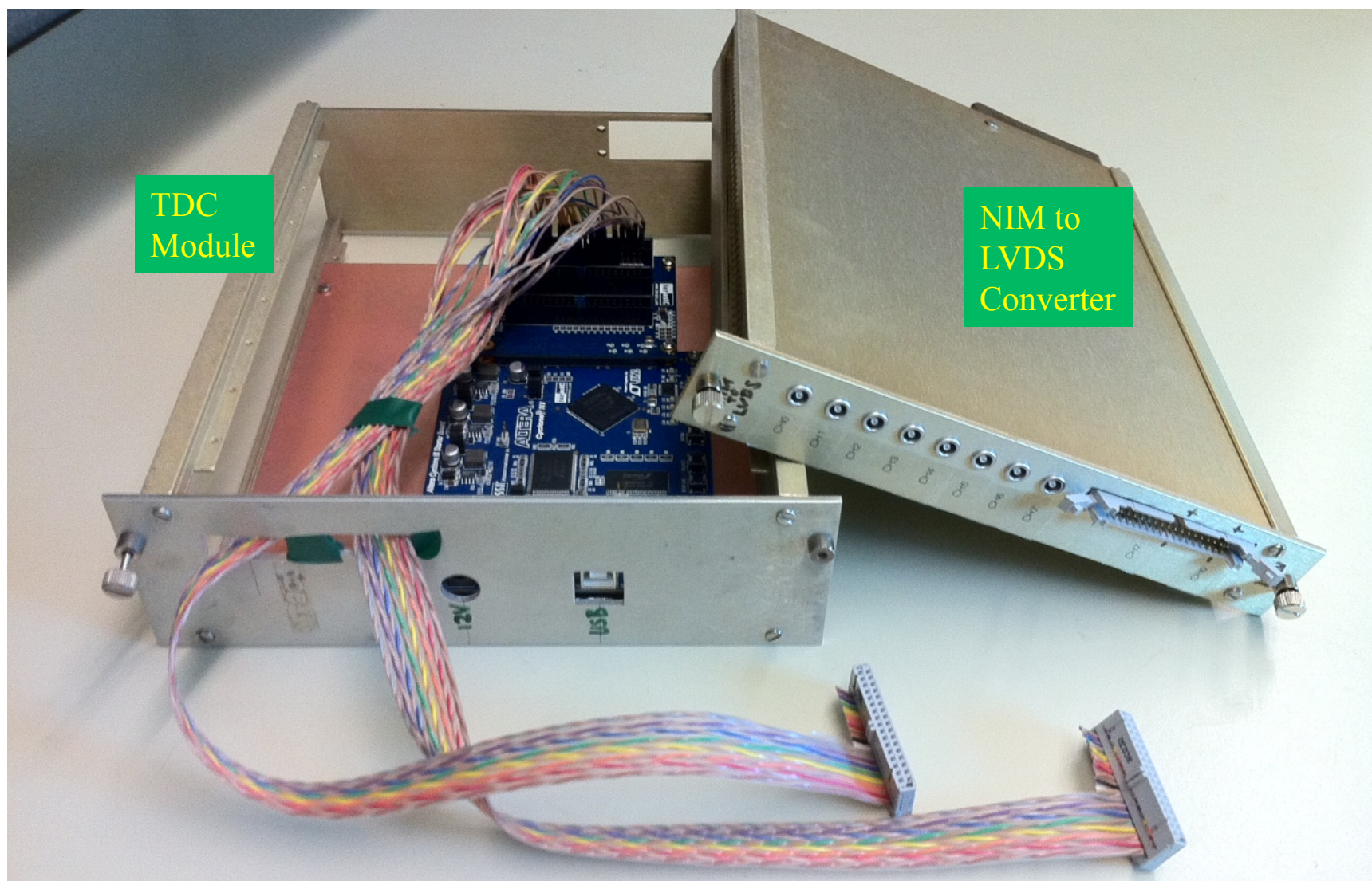
Altera Cyclone III Starter Kit (\$211+\$50)

FPGA: EP3C25F324C6N (\$73.90)

32 channel: 30 ps (25 ps with linear power supply)

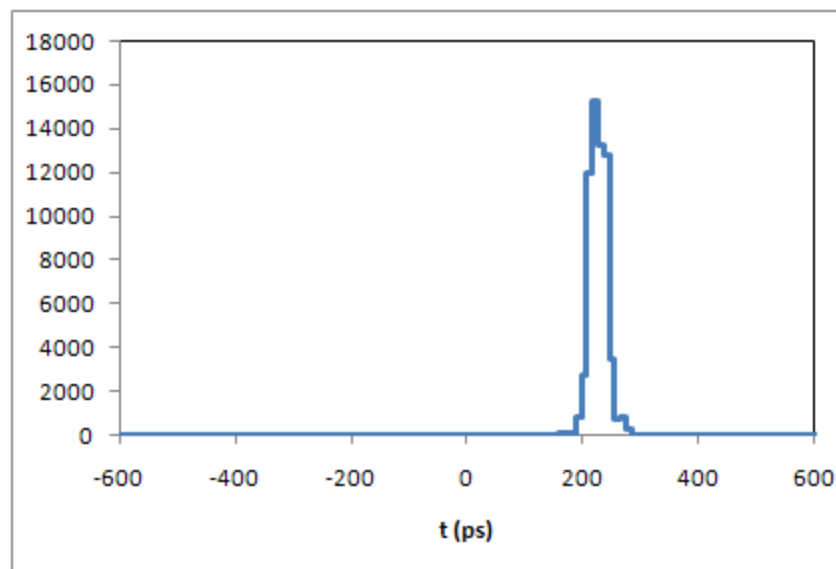
27 mW/channel

# Test Setup



# Output Raw Data and Typical Delta T Histogram Between Two Channels

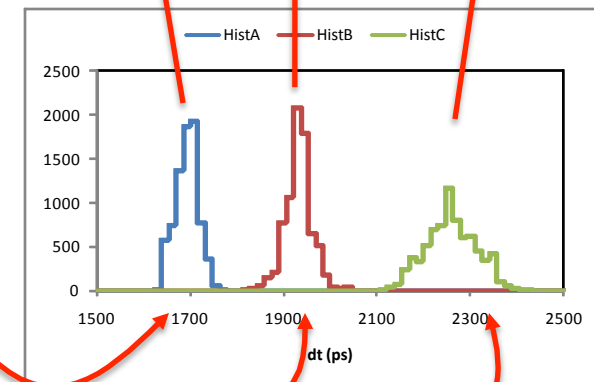
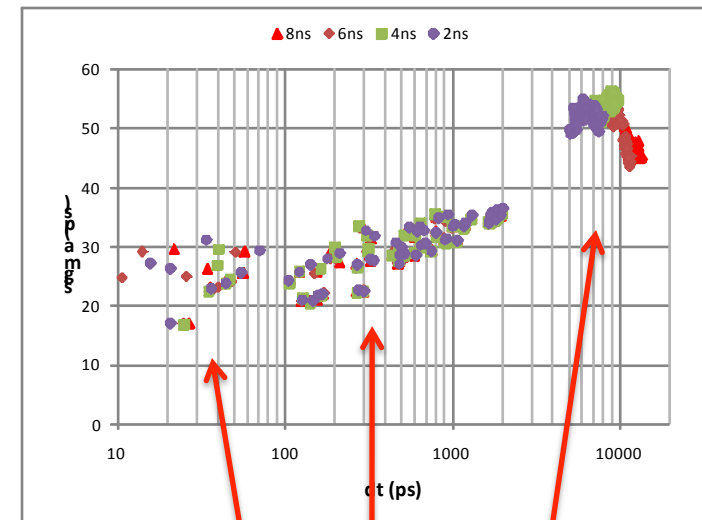
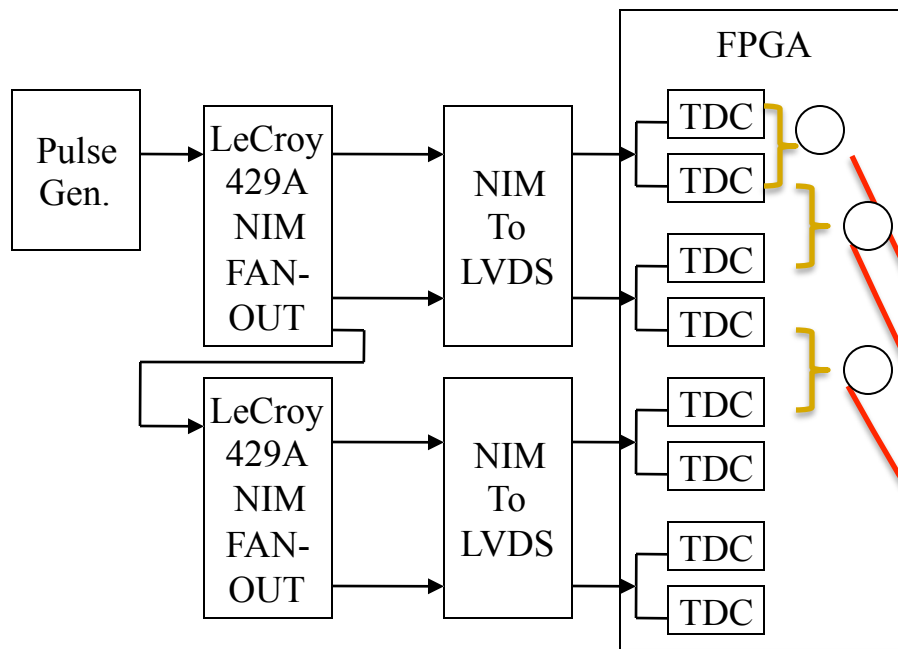
00003C  
C064A6  
F064B8  
C07CA4  
F07CB4  
C094A0  
F094B0  
C0AC9C  
F0ACAC  
C0C497  
F0C4A8  
C0DC91  
F0DCA2



■ RMS of this histogram is 25 ps.

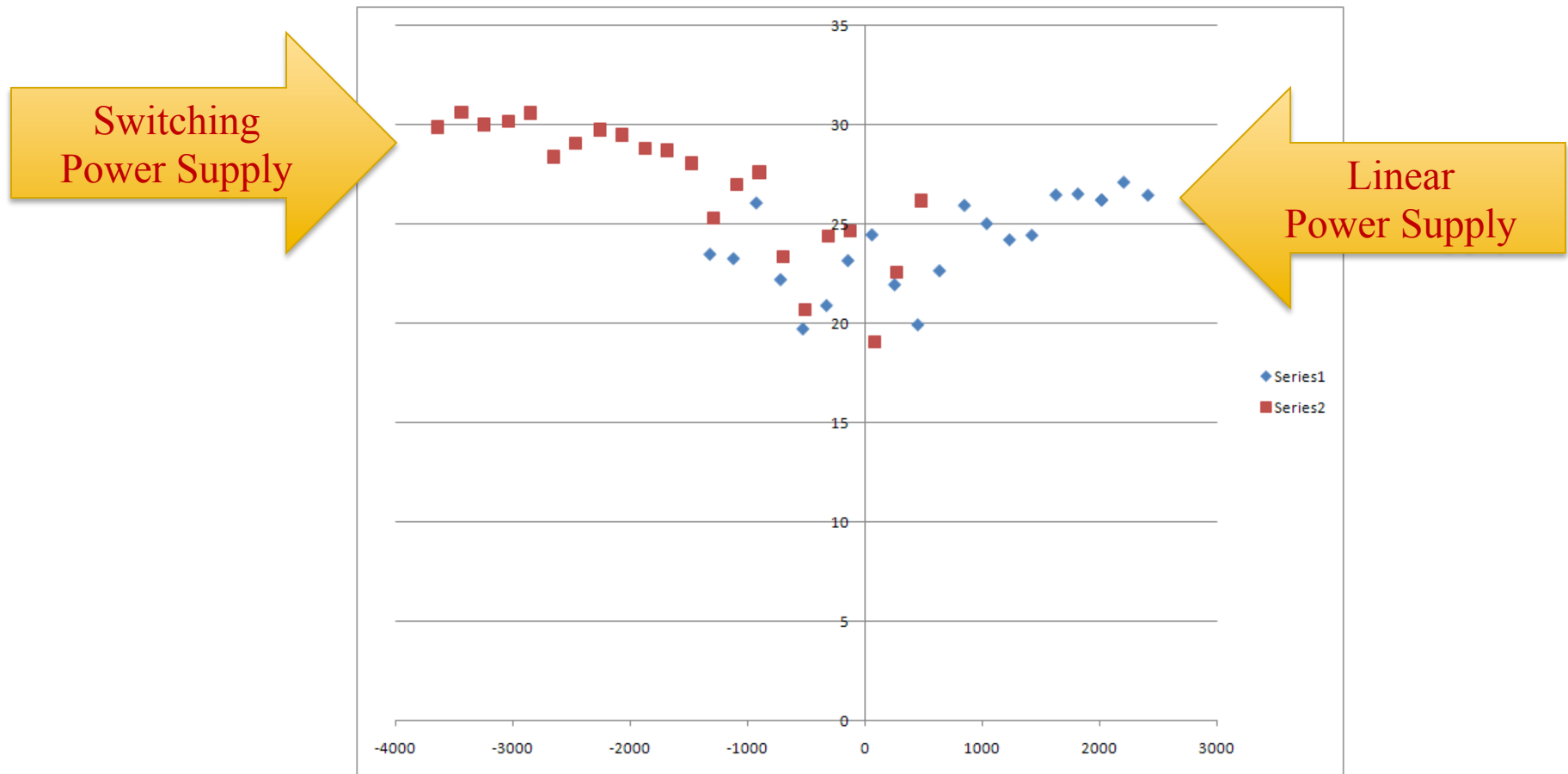
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH[3..0]				Coarse Time, LSB=4ns, TC[11..0]=96--4095, full range = 4000*4ns=16us												Fine Time, LSB=4000 ps/256=15.625ps							

# Delta T Between NIM Inputs



- TDC channels internally ganged together has smallest standard deviation of time differences.
- Typical channel pairs sharing same fan-out unit has 30 ps RMS.
- Timing jitters of the fan-out units add to the measurement errors.

# Time Measurement Errors Due to Power Supply Noise

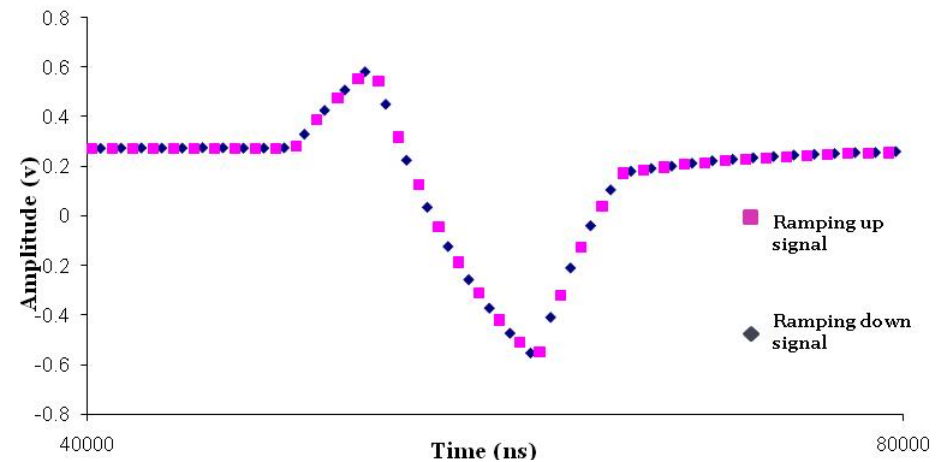
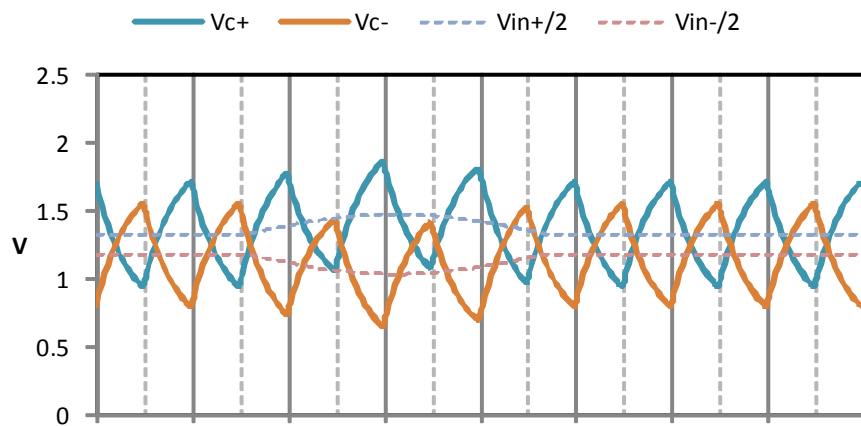
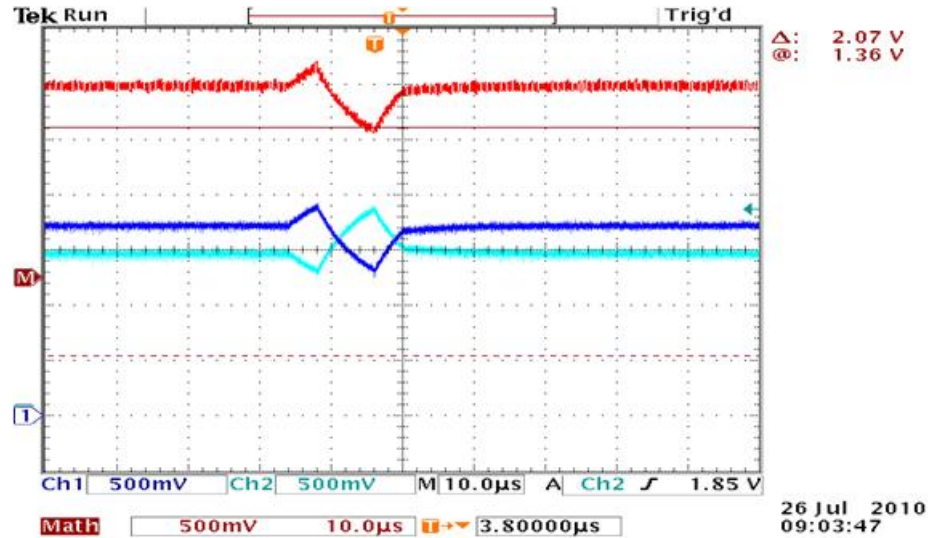
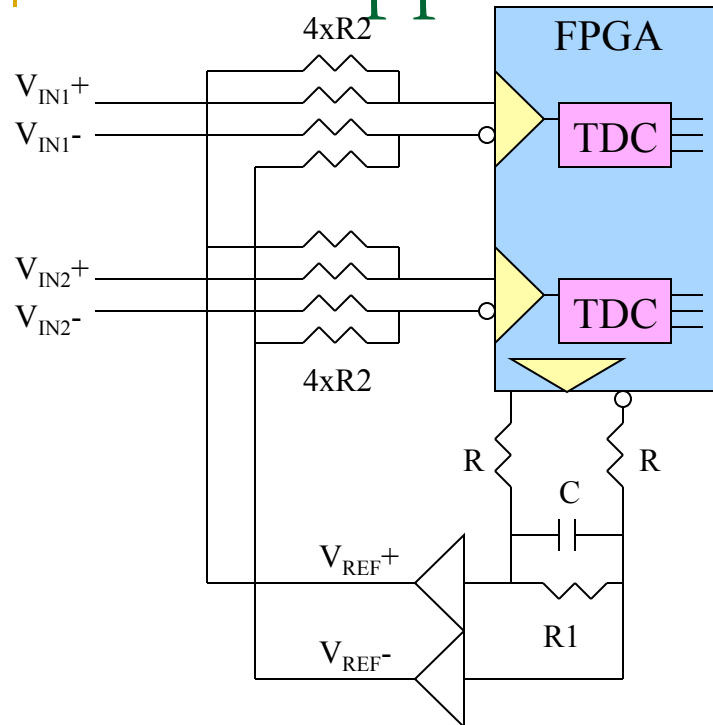


- Typical RMS resolution is 25-30 ps.
- Measurements with cleaner power (diamonds) is better than noisy power (squares).

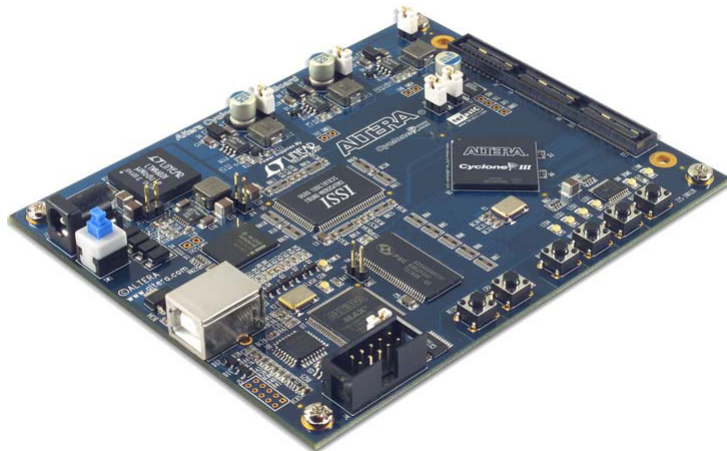
## Specifications

RMS Resolution (Delta T between two channels)	25 to 30 ps
Same channel re-hit time interval	64 ns
Temporary buffer capacity	128 hits/(4 ch)/(16 us)
LVDS output port rate:	250 M bits/s/port
Output capacity in each LDVS output port:	128 hits/(16 ch)/(16 us)
Number of LVDS output ports:	1, 2, 3, 4/(16 ch)
Power Consumption (Core only)	9.3 mW/channel
Power Consumption (Total)	27 mW/channel

# Other Applications: Single Slope ADC



## If You Want to Try

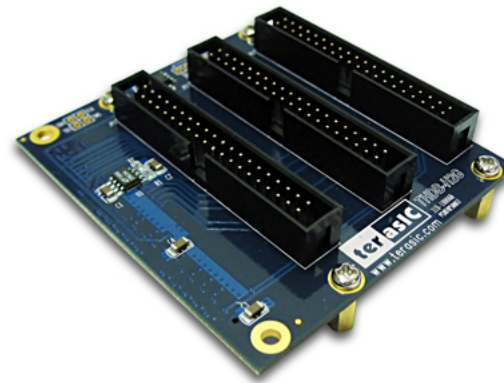


[www.altera.com](http://www.altera.com)

DK-START-3C25N

Cyclone III FPGA Starter Kit

\$211



[www.altera.com](http://www.altera.com)

THDB-H2G

(HSMC to GPIO Daughter Board)

\$50

- The FPGA on the Starter Kit is fairly powerful.
- More than 16 pairs LVDS I/O can be accessed via the daughter card.
- FPGA can fit 32 channels but implementing 16 channels is more practical given the I/O pairs.
- TDC data are stored in the RAM on the board and can be readout via USB.
- A good solution for small experiment systems as well as student labs.

An aerial photograph of a golf course. The course features a large, winding green fairway and a prominent sand trap in the center. A clubhouse with a distinctive white, curved roof is situated on the right side of the image. The surrounding area includes fields, trees, and some residential buildings. A yellow line is drawn across the top of the image.

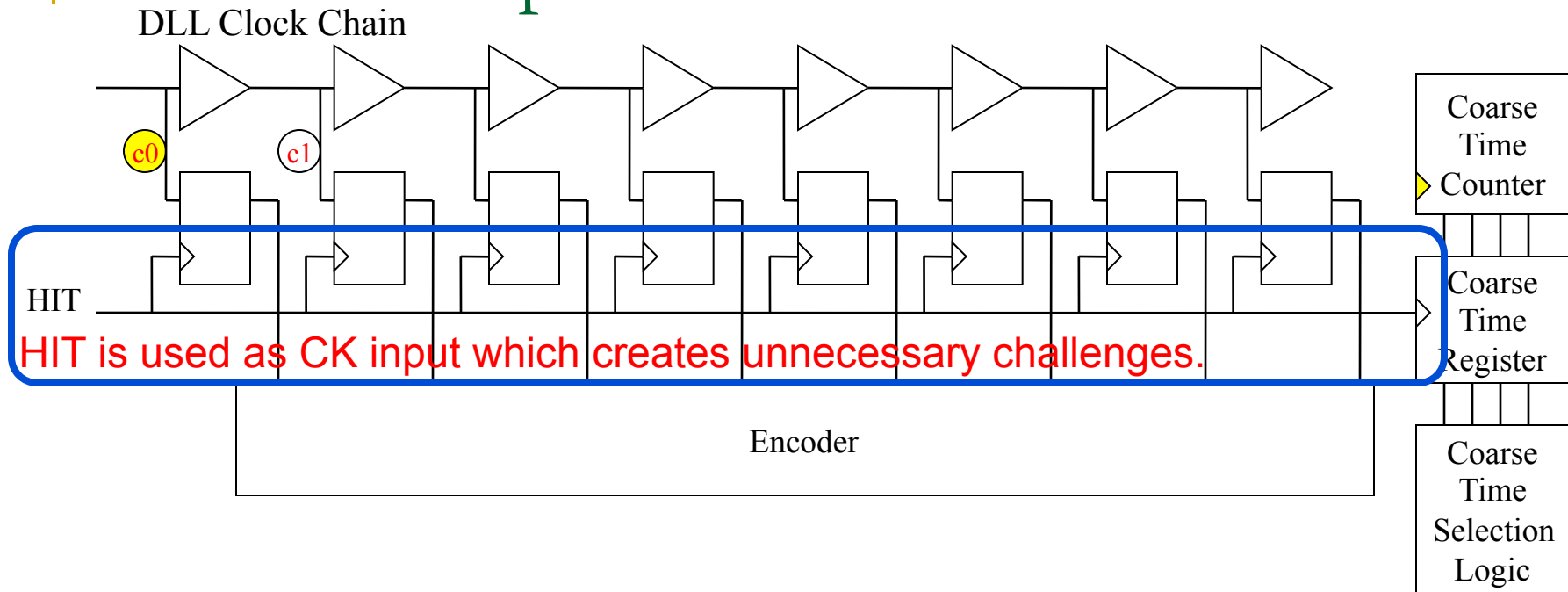
The End

Thanks

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# Timing Uncertainty Confinement

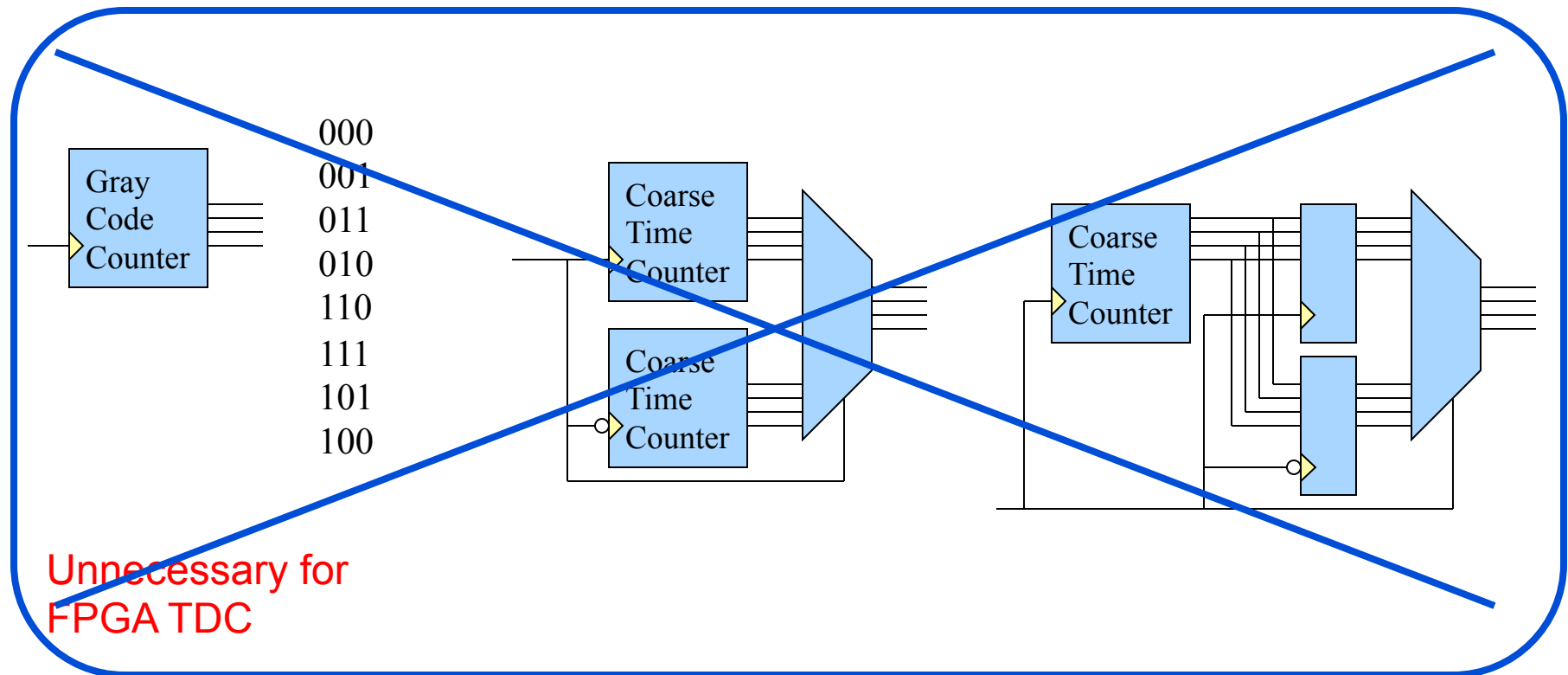
# Historical Implementation in ASIC TDC



Unnecessary Challenges = Extra Efforts + Reduced Performance

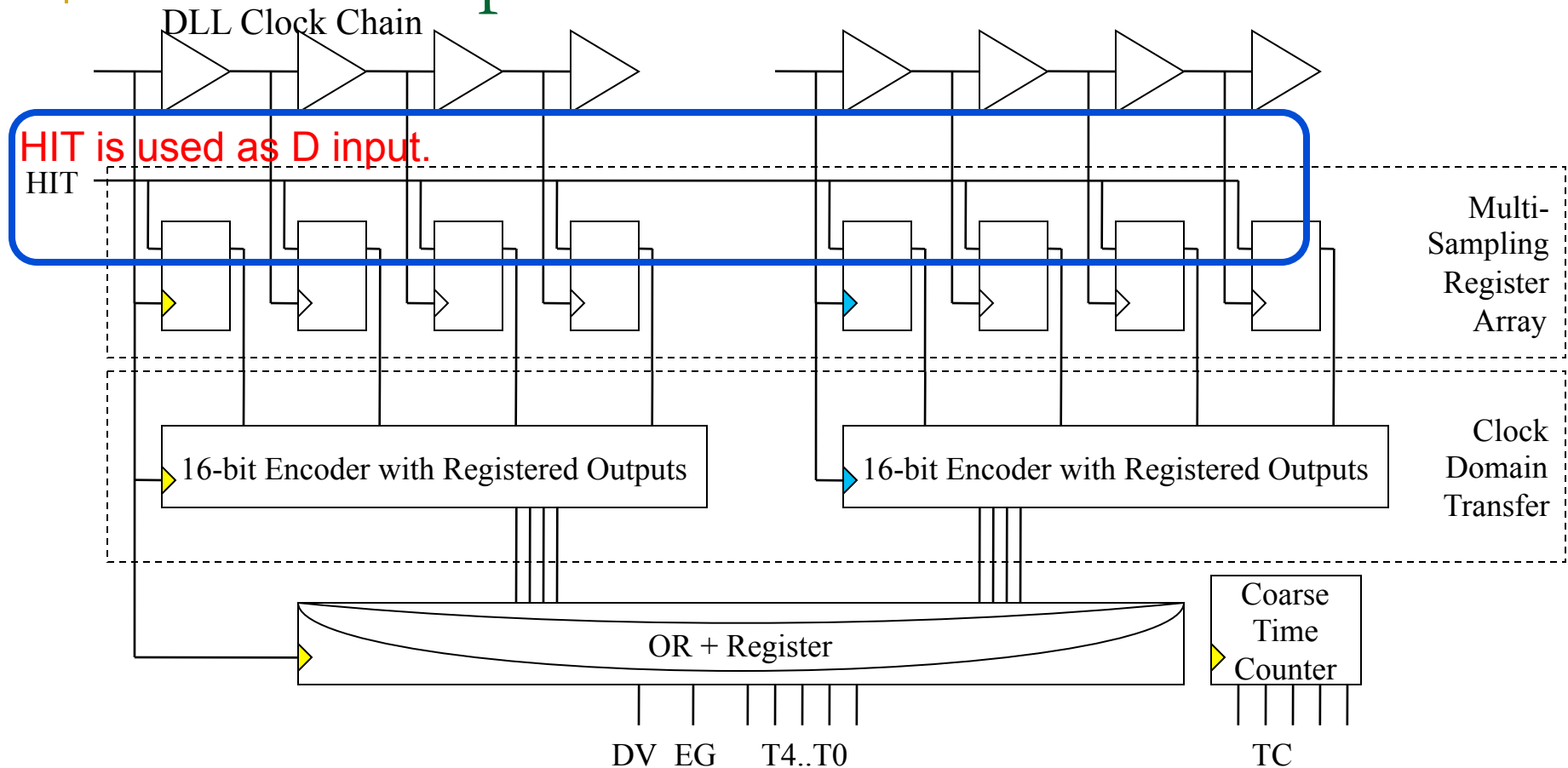
- Deadtime is unavoidable.
- Coarse time recording needs special care.
- Two array + encoder sets are needed for raising edge and falling edge.
- The register array must be reset for next event.
- The encoder must be re-synchronized with system clock in order to interface with readout stage.

# Unnecessary Challenges



- In history, Gray code counters, double counters and dual registers + MUX are found in ASIC TDC coarse time counter schemes.
- These are unnecessary if the TDC is designed appropriately.
- In FPGA, a plain binary counter is sufficient.

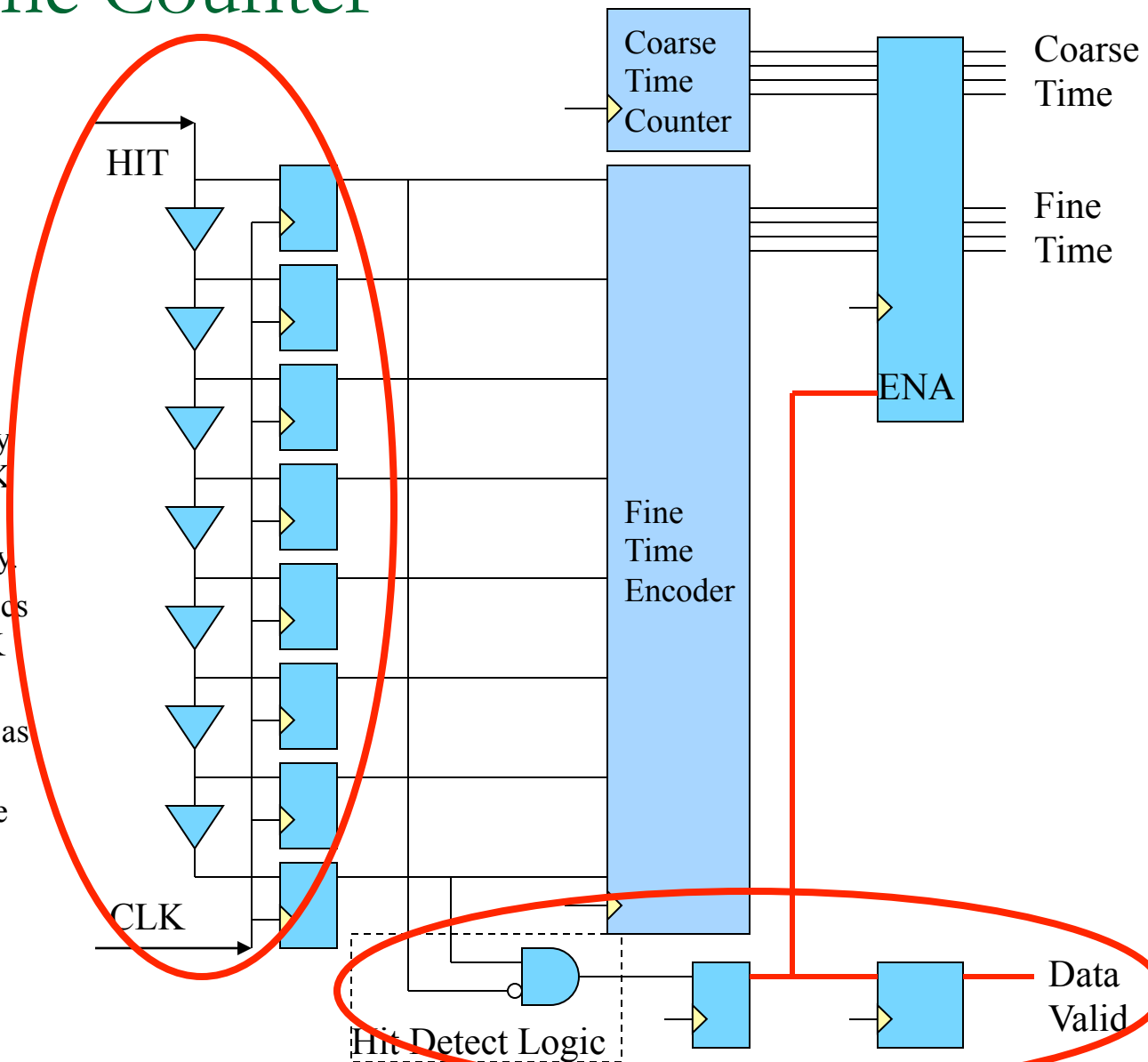
# A Better Implementation



- Deadtimeless operation is possible.
- No special care is needed for coarse time.
- Both raising and falling edges are digitized with a single array + encoder set.
- No resetting is needed for the register array.
- The output is synchronized with the system clock and is ready to interface with readout stage.

# Coarse Time Counter

- The timing uncertainty between HIT and CLK is confined in the sampling register array.
- All the remaining logics are driven by the CLK signal.
- No special cares such as Gray code counter is needed for coarse time counter.



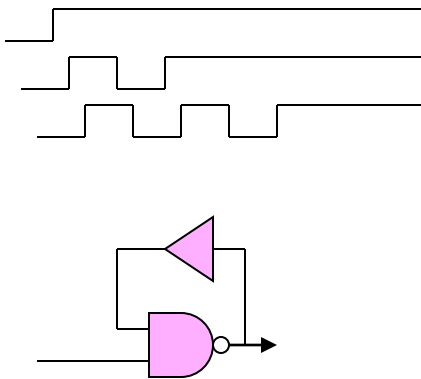
# Comparison

<b>Historical Scheme:</b> HIT-> CK; (c0..c31)->D;	<b>Preferable Scheme:</b> HIT-> D; (c0..c31)->CK;
Deadtime is unavoidable.	Deadtimeless operation is possible.
Coarse time recording needs special care.	No special care is needed for coarse time.
Two array + encoder sets are needed for raising edge and falling edge.	Both raising and falling edges are digitized with a single array + encoder set.
The register array must be reset for next event.	No resetting is needed for the register array.
The encoder must be re-synchronized with system clock in order to interface with readout stage.	The output is synchronized with the system clock and is ready to interface with readout stage.

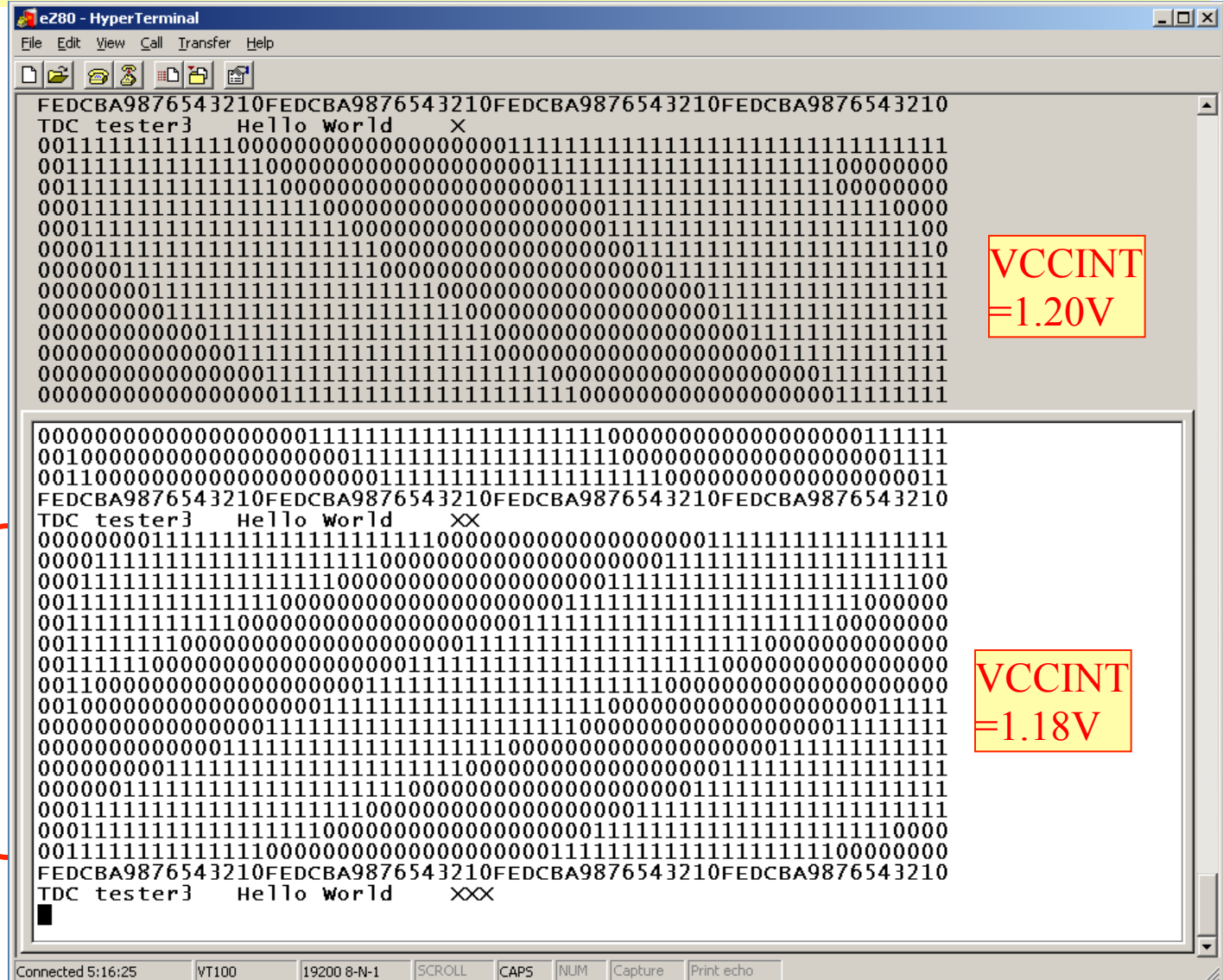
# More Measurements

- Two measurements are better than one.
- Let's try 16 measurements?

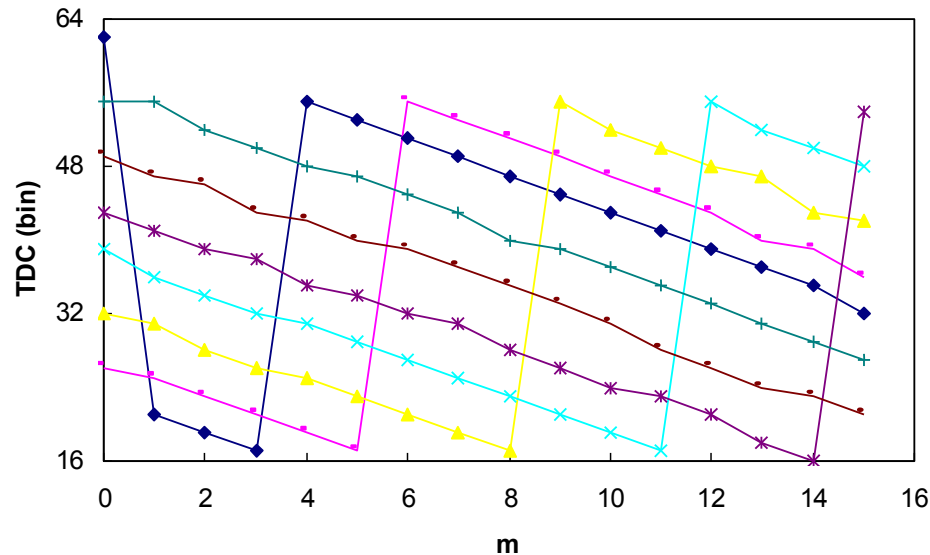
## Wave Union Launcher B: *16 Measurements/hit*



1 Hit  
16 Measurements  
@ 400 MHz



# Delay Correction

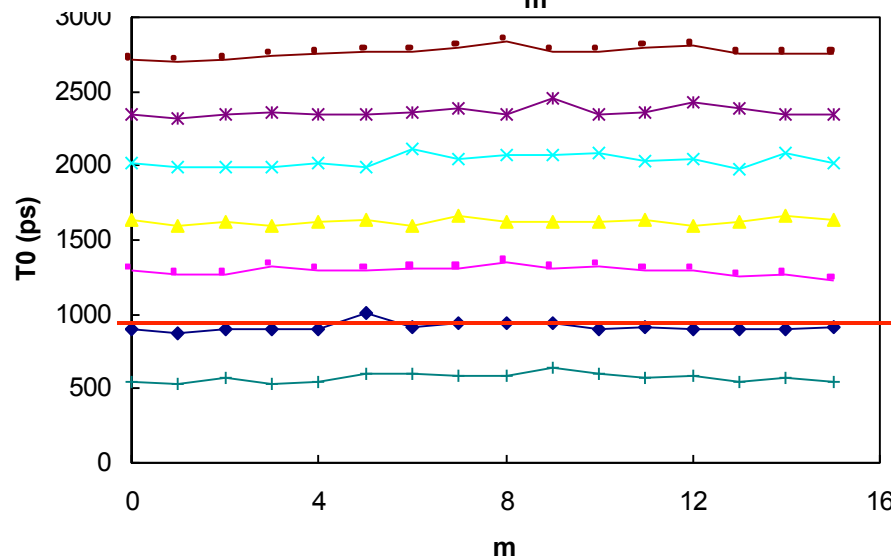


The raw data contains:

- U-Type Jumps: [48-63]→[16-31]
- V-Type Jumps: other small jumps.
- W-Type Jumps: [16-31]→[48-63]

## Delay Correction Process:

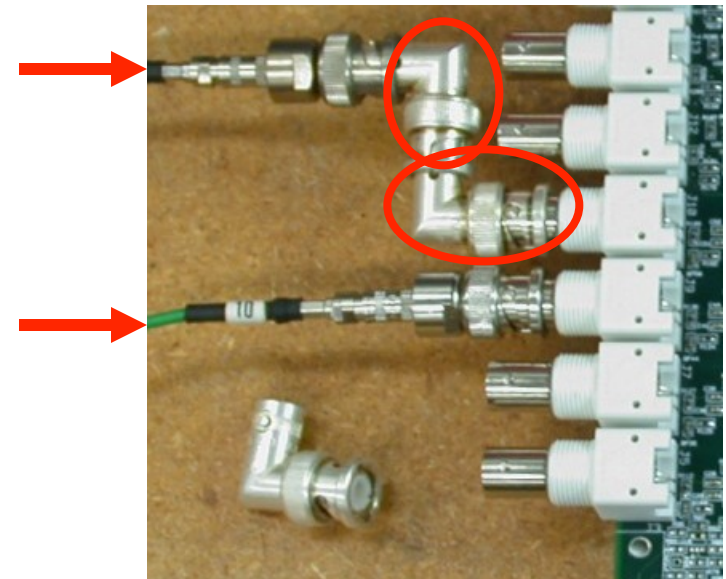
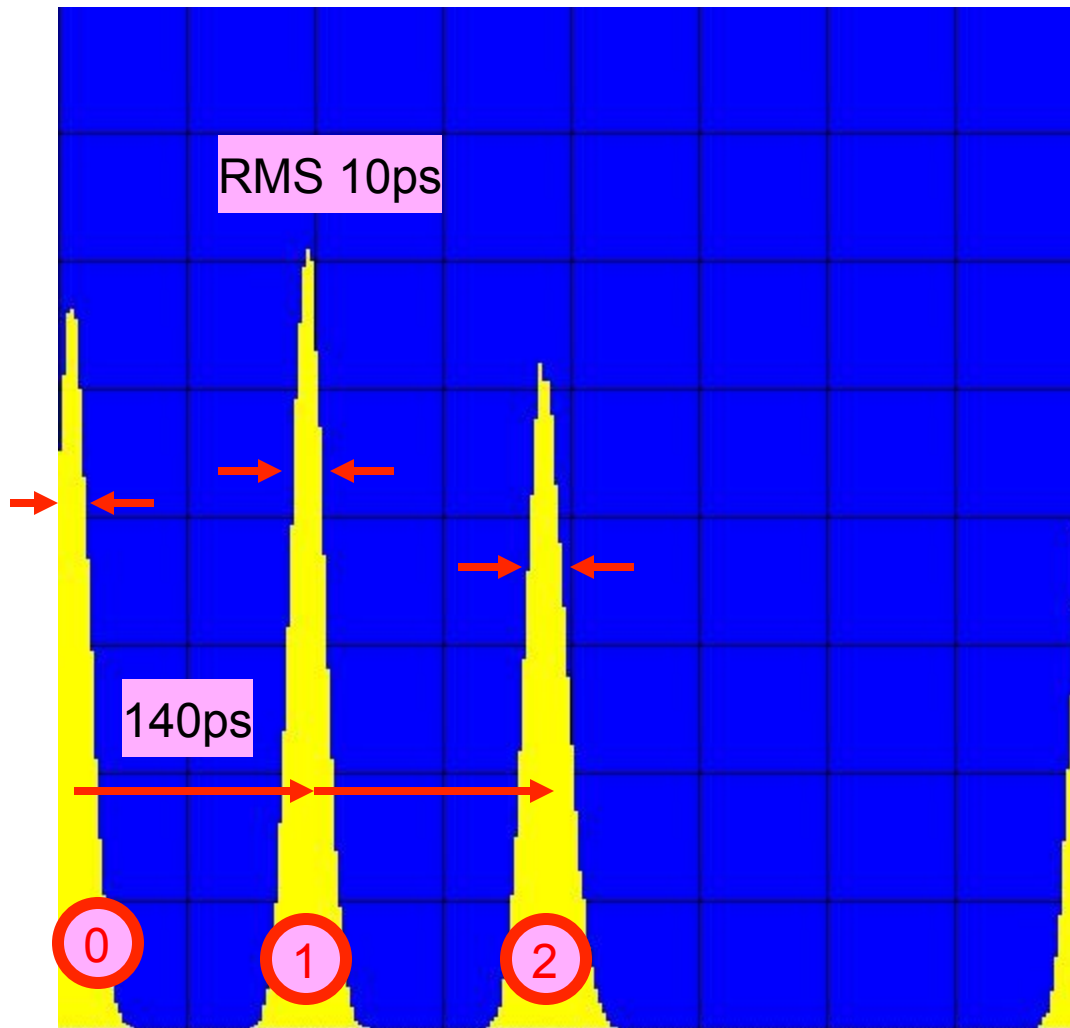
- Raw hits TN(m) in bins are first calibrated into TM(m) in picoseconds.
- Jumps are compensated for in FPGA so that TM(m) become T0(m) which have a same value for each hit.
- Take average of T0(m) to get better resolution.



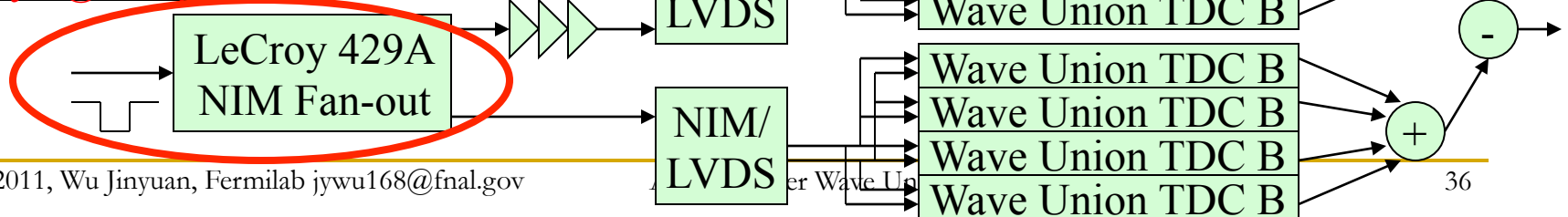
$$t_{0av} = \frac{1}{16} \sum_{m=0}^{15} t_0(m)$$

The processes are all done in FPGA.

## Test Result NIM Inputs

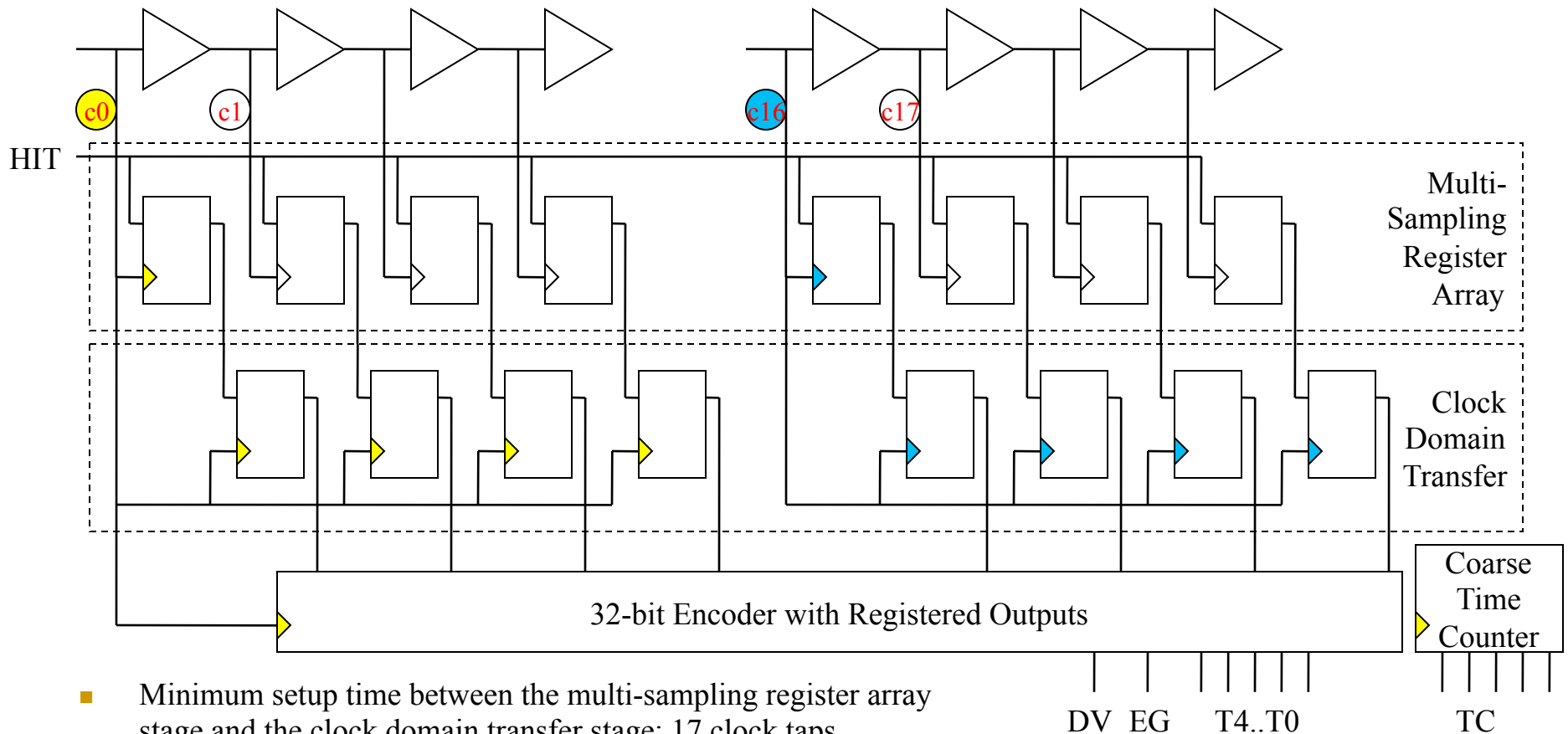


BNC adapters to add  
delays @ 140ps step.



# A Preferable Scheme

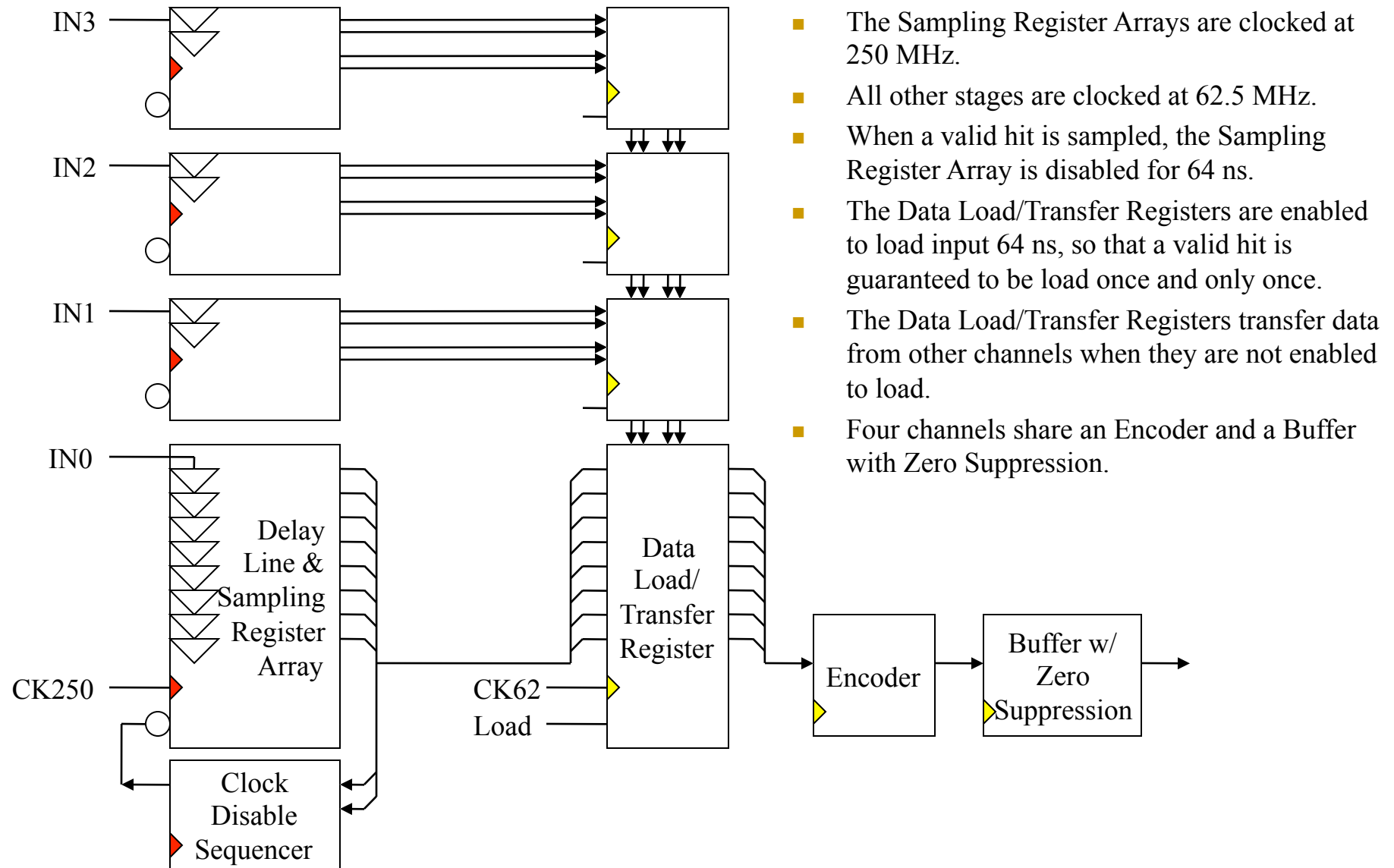
## DLL Clock Chain



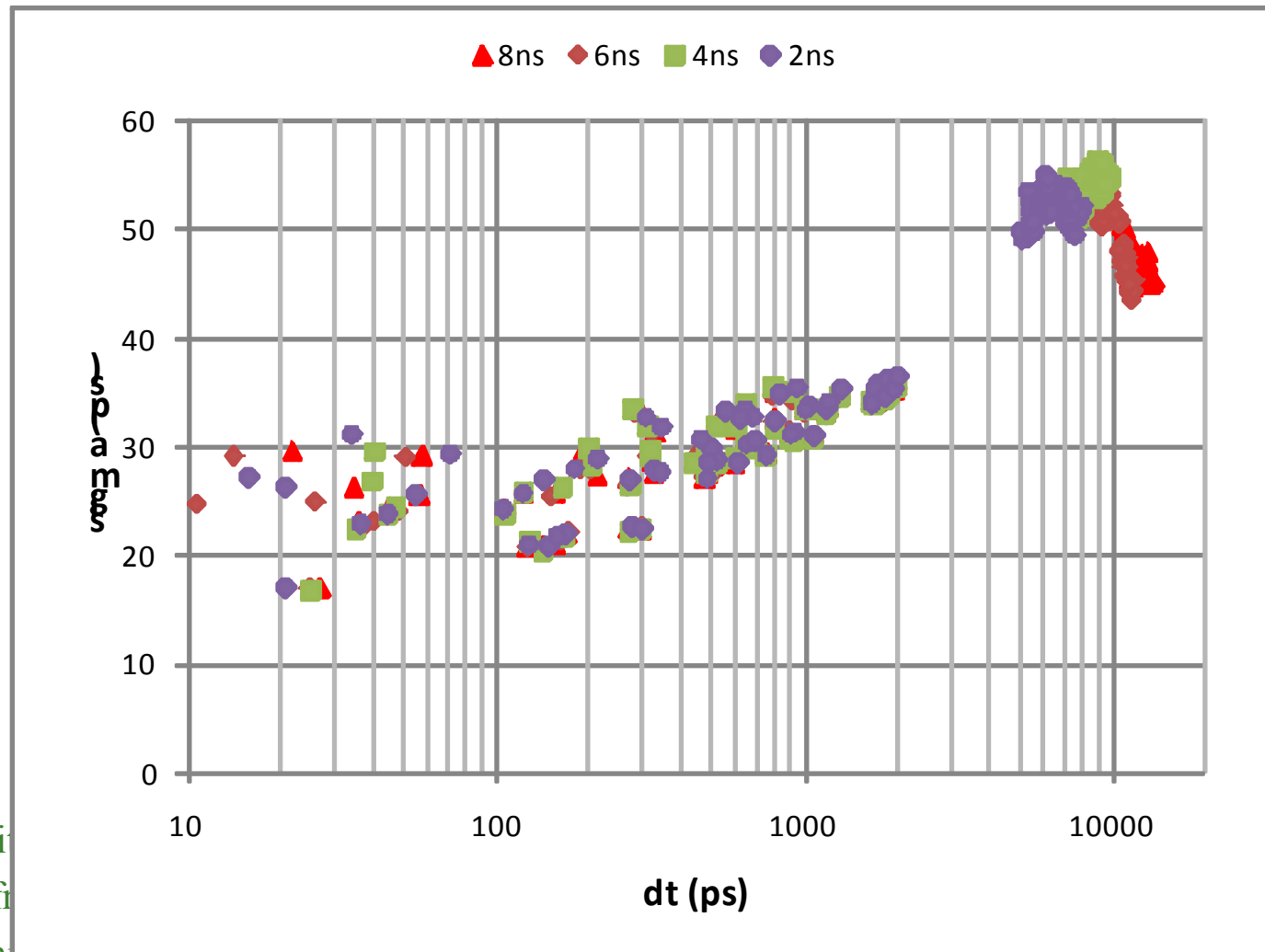
- Minimum setup time between the multi-sampling register array stage and the clock domain transfer stage: 17 clock taps.
- Setup time between the clock domain transfer stage and the encoder register: 32 or 16 clock taps.
- All outputs including TC are aligned with c0.
- Supports both raising and falling edges.

EG: Edge, =1: Raising or =0: Falling.  
 T4..T0: Time.  
 DV: Data Valid, =1 Valid edge detected.  
 It is used as PUSH signal for FIFO or  
 Write Enable for other memory buffers.

# Low Power Design Practice: Clock Speed

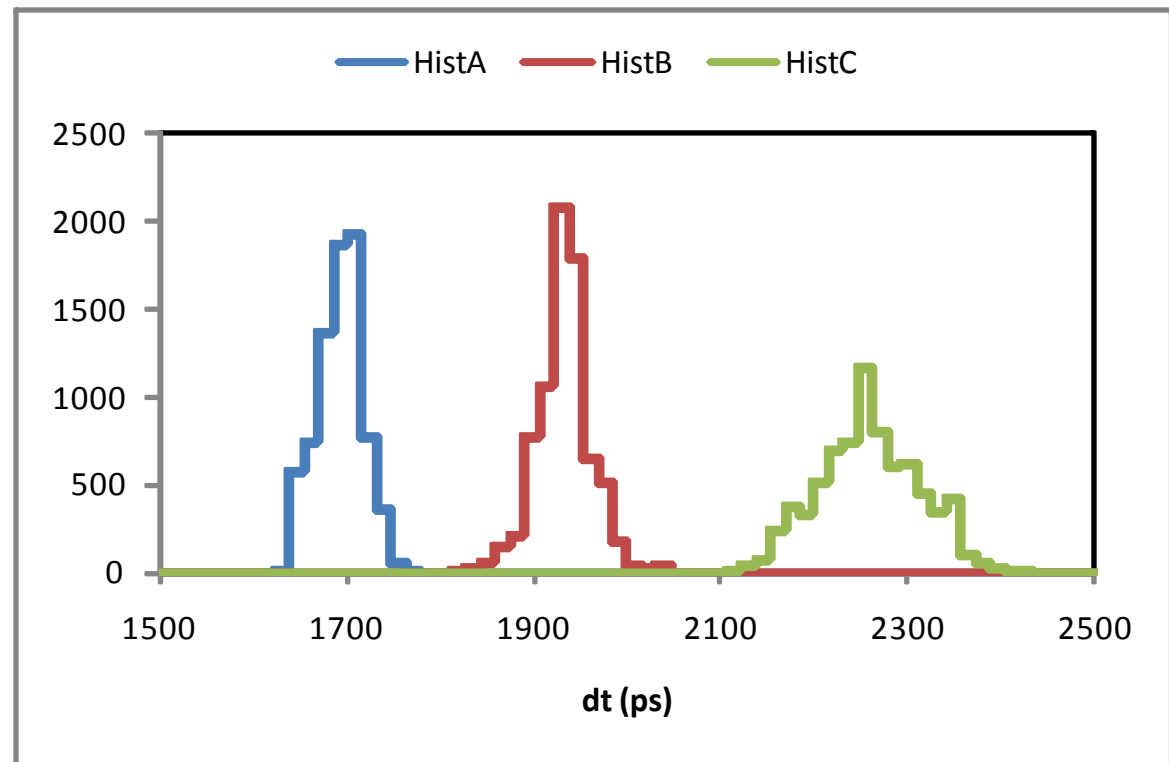


# Test Setup



- The hi
- Data fi
- Raw hit times are converted to time through automatic calibration block.
- Data from all 16 channels are buffered and sent out via 4 pairs of LVDS ports @250 M bits/s.

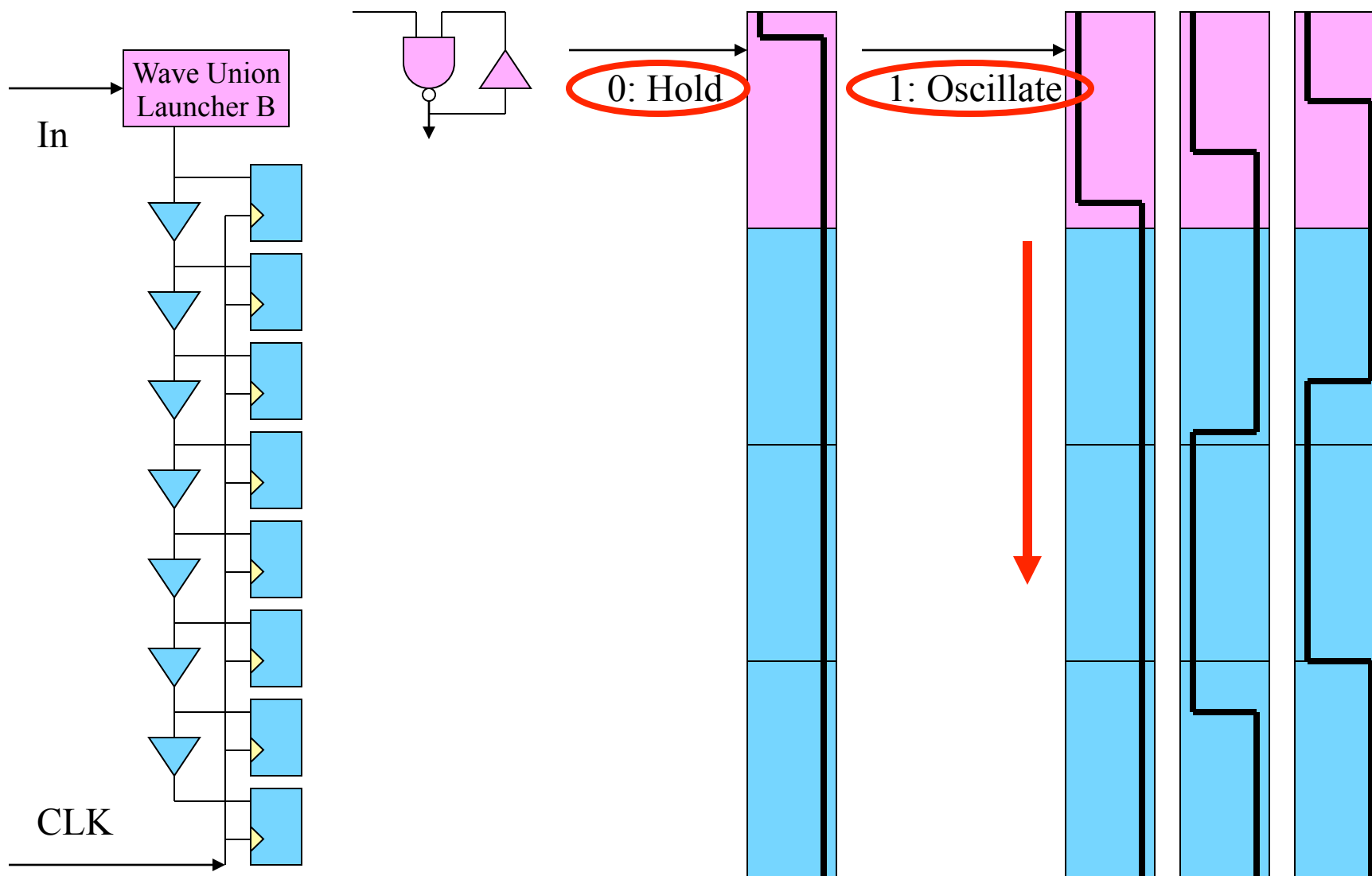
# Test Setup



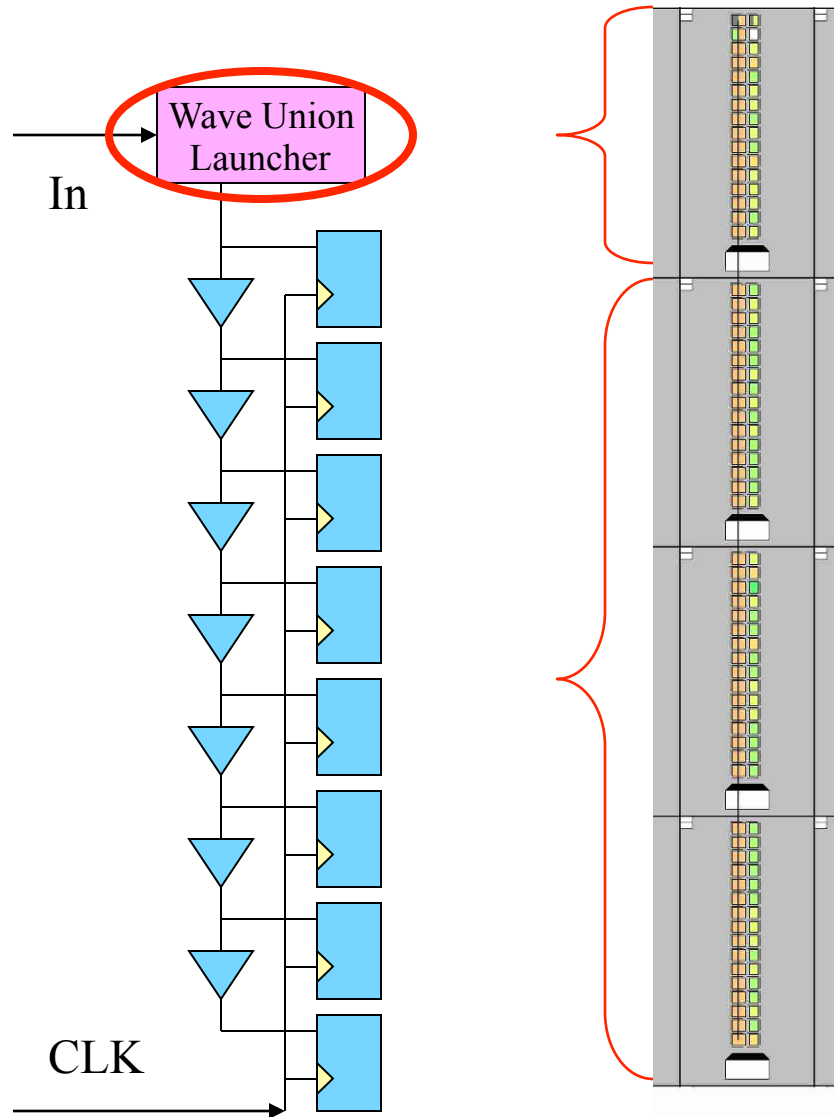
TDC +  
Encoder

- The hit time for each of the 16 channel inputs is digitized and encoded.
- Data from 4 channels are buffered and data from 4 groups of 4 channels are merged together.
- Raw hit times are converted to fine time through automatic calibration block.
- Data from all 16 channels are buffered and sent out via 4 pairs of LVDS ports @250 M bits/s.

# Wave Union Launcher B



# Cell Delay-Based TDC + Wave Union Launcher



The wave union launcher creates multiple logic transitions after receiving a input logic step.

The wave union launchers can be classified into two types:

- Finite Step Response (FSR)
- Infinite Step Response (ISR)

This is similar as filter or other linear system classifications:

- Finite Impulse Response (FIR)
- Infinite Impulse Response (IIR)

# Wave Union?



Photograph: Qi Ji, 2010